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MICROMINIATURE SIGNAL CONDITIONER

FINAL REPORT

REPORT NO. 05183-6003-R000 22 MAY 1967

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER

Contract No. NAS9-4640

TRW SYSTEMS GROUP

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NASA Offices and Approved Contractors Only

TRW SYSTEMS GROUP

FOREWORD

This work was performed by the Microelectronics Center of TRW Systems Group, TRW Inc., One Space Park, Redondo Beach, California, under NASA Contract No. NAS9-4640, "Microminiature Signal Conditioner." This report covers work conducted from July, 1965 through March, 1967 and is identified as Report No. 05183-6003-R000 by the Contractor. Members of the Technical Staff include D. R. Breuer, Project and Design Engineer, and J. L. Buie, Head, Microelectronics Research and Development Section.

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1. INTRODUCTION

1.1 GENERAL DESCRIPTION

This report describes the work performed under contract NAS9-4640 to develop an

a. ultra-low-drift monolithic instrumentation amplifier, and a

b. microelectronic power source.

The differential amplifier serves as a basic building block in the advanced microelectronic space telemetry system developed under contract NAS9-5293. This compatible monolithic low-level amplifier offers characteristics competitive with state-of-the-art discrete component chopper amplifiers. For instance, the circuit provides ultra-low dc offset drifts (from 0.1 to 0.5 $\mu V/^{o}C$ referred to the input, over $-35^{o}C$ to $+95^{o}C$ temperature range), high voltage gain, high input impedance, and high common-mode rejection. The switching problems associated with chopper amplifiers are, however, absent. This direct-coupled amplifier stabilizes rapidly with gated supply power, allowing power to be sequentially applied in an application such as the Power Programmer system developed under contract NAS9-5293.

Development of this amplifier was begun under contract NAS9-3410 and completed under the contract being reported, NAS9-4640. The NAS9-3410 configuration of six monolithic compatible integrated circuit die, plus MOS roll-off capacitors, was reduced to two monolithic integrated circuit die plus capacitors under NAS9-4640. This increases the reliability and economic producibility of the circuit.

The microelectronic power source was developed under NAS9-4640. This function converts a 22 to 32 volt battery input into three regulated voltages, a 10.000 ± 0.050 volt transducer excitation and a $\pm$ 15 volt

amplifier supply. The power source includes a microminiature transformer-isolated power converter and three monolithic dielectrically isolated compatible integrated circuit post voltage regulators.

Hardware shipment includes:

a. Five (5) integrated circuit amplifiers, gain of 1,000,

b. Five (5) integrated circuit amplifiers, gain of 50,

c. Five (5) micromininiature power sources, and

d. One (1) module test unit.

1.2 SPECIFICATIONS

The contract specifications are included in Appendix A. Additional amplifier specifications and application notes are provided in Appendices B and C, respectively. Test data is included in Section 5.

2. AMPLIFIER

2.1 DESIGN PRINCIPLES

2.1.1 General

The following techniques are used to produce the monolithic amplifier specified by this contract.

a. The performance specifications of the amplifier developed under this contract demand preciseness of the following characteristics.

   1) Gain accuracy (0.2% initial setting)
   2) Common-mode rejection (100 dB at dc)
   3) DC offset (10 μV referred to input)
   4) DC offset temperature drift (0.2 $\mu V/^{o}C$ referred to input)

   The standard monolithic integrated circuit approach of selecting die to meet a given criteria is clearly inadequate, due to the degree of accuracy required simultaneously in four parameters. Post-fabrication adjustment of resistor values is necessary, in addition to die selection, to adjust the amplifier performance in each of the stated parameters. (See Section 4.)

b. The compatible integrated circuit structure, which incorporates cermet thin film resistors evaporated on a semiconductor substrate, is required to provide the resistor stability dictated by the performance specifications. (See Section 4.)

c. Overall emitter feedback is required to allow the specifications of high closed-loop gain (1000), high input impedance (50 K ohms), and low dc offset drift (0.2 $\mu V/^{o}C$ referred to input) to be simultaneously met. (See Section 2.1.2.)

d. A special drift-offset control circuit is used to compensate for the inherent offset and drift of the amplifier and simultaneously maintain high common-mode rejection. (See Section 2.1.3.)

2.1.2 Basic Amplifier

Overall negative feedback from the output back to the emitter of the input transistors, as shown in Fig. 2-1, offers gain accuracy, low dc drift,

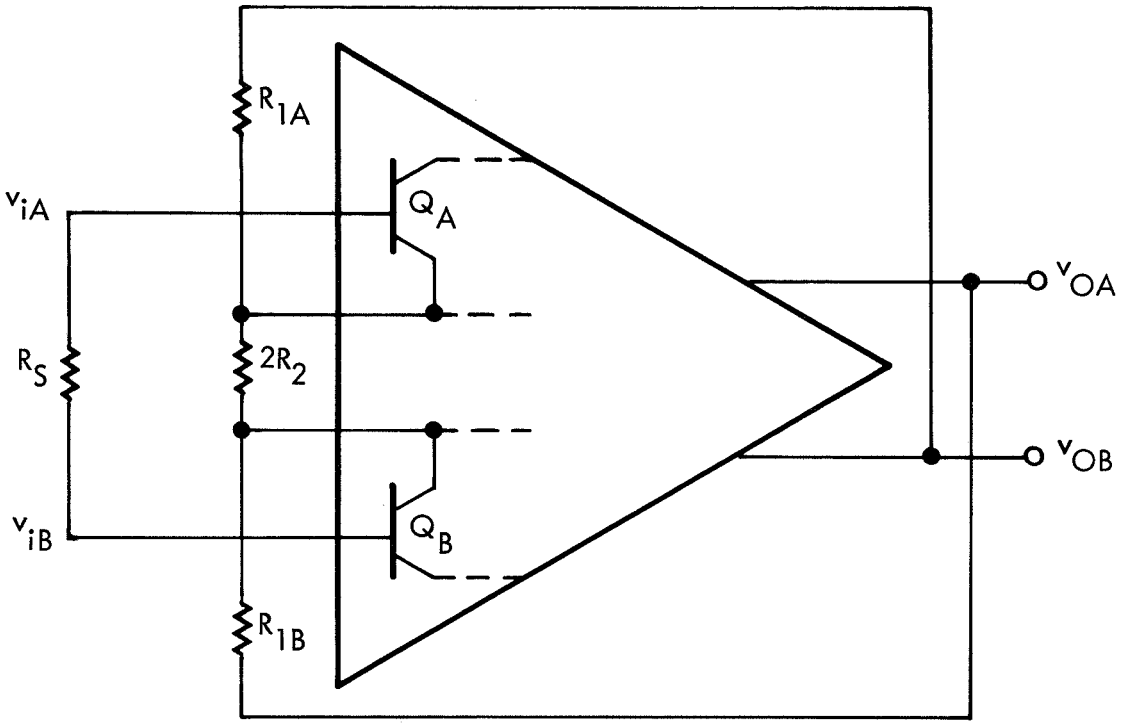

Fig. 2-1. Overall Emitter Feedback

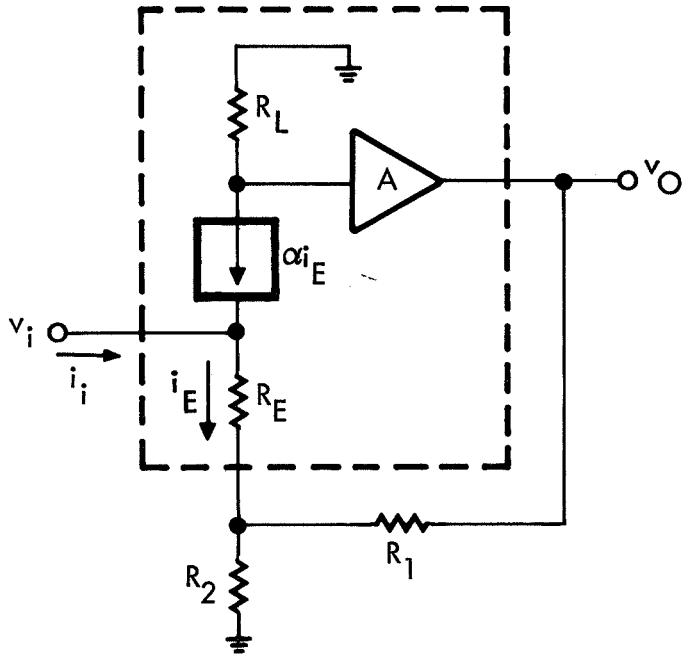

Fig. 2-2. Differential Equivalent Circuit

minimum source dependence, high input impedance, and low output impedance. This emitter-type feedback is therefore preferred for this application.

This choice of overall feedback is best understood by examining the compliment connection, base-type feedback, which is typically used for operational amplifiers. It is unacceptable in this direct-coupled amplifier application because of the high input impedance and low dc drift specifications.

Assuming a perfectly balanced, symmetrical configuration, a differential-mode equivalent half circuit[1] can be drawn, as in Fig. 2-2, to illustrate the differential-mode performance. The input stage is shown separate from the remaining portion of the amplifier. Analysis yields

$$\frac{v_o}{v_i} = \left[\frac{R_1 + R_2}{R_2}\right] \times \left[\frac{1}{1 - \frac{1}{A_T}\left[\frac{R_1 + R_2}{R_2} + \frac{R_1}{R_E}\right]}\right], \tag{2-1}$$

where $$R_E = r_E + \frac{R_S + r'_B}{\beta} \tag{2-2}$$

$$r_E \equiv \text{emitter diffusion resistance of input transistors,} \tag{2-3}$$

$$R_S \equiv \text{source impedance,} \tag{2-4}$$

$$r'_B \equiv \text{base spreading resistance,} \tag{2-5}$$

$$A_T \simeq \alpha \times \frac{R_L}{R_E} \times A, \text{ and} \tag{2-6}$$

$$A \equiv \text{open loop gain exclusive of input stage gain} \tag{2-7}$$

---

[1] R. D. Middlebrook, Differential Amplifiers (John Wiley and Sons, Inc., New York)

If A_T is very large, the closed loop gain becomes

$$\frac{v_o}{v_i} \simeq \frac{R_1 + R_2}{R_2} \tag{2-8}$$

For non-negligible A_T, the closed loop voltage gain expressed by Eq. 2-1 deviates from the ideal gain expressed by Eq. 2-8, by the following percentage error

$$(\%\ \text{error in}\ \frac{v_o}{v_i}) = \frac{1}{A_T} \times \left[\frac{R_1 + R_2}{R_2} + \frac{R_1}{R_E}\right] \times 100. \tag{2-9}$$

Note that the source impedance, R_S, does not appear in Eq. 2-8, but only within R_E and A_T in the error term of Eq. 2-9. Examination of this latter equation reveals that a variation in R_S has a negligible effect on the closed loop gain. Substitution of Eq. 2-2 and Eq. 2-6 into Eq. 2-9 provides an expression for the % error of $\frac{v_o}{v_i}$ in terms of R_S, and is given as

$$(\%\ \text{error in}\ \frac{v_o}{v_i}) = \left[\frac{R_S}{\alpha\beta R_L A} \times \frac{R_1 + R_2}{R_2} + \frac{r'_B}{\alpha\beta R_L A} \times \frac{R_1 + R_2}{R_2} + \frac{r_E}{\alpha R_L A} \times \frac{R_1 + R_2}{R_2} + \frac{R_1}{\alpha R_L A}\right] \times 100 \tag{2-10}$$

The change in the % error of $\frac{v_o}{v_i}$ for a change in source resistance is then given by

$$\Delta(\%\ \text{error in}\ \frac{v_o}{v_i}) = \left[\Delta R_S \times \frac{1}{\alpha\beta R_L A} \times \frac{R_1 + R_2}{R_2}\right] \times 100 \tag{2-11}$$

Substituting the following values into Eq. 2-11

$$\Delta R_S = 1000 \text{ ohms variation}$$

$$\alpha = 0.98$$

$$\beta = 50$$

$$R_L = 50{,}000 \text{ ohms}$$

$$A \geq 5000$$

$$\frac{R_1 + R_2}{R_2} = 1000$$

yields

$$\Delta(\% \text{ error in } \frac{v_o}{v_i}) = 0.01\%, \tag{2-12}$$

a negligible quantity for the case considered.

Also note that the emitter current level of the input transistor pair affects the closed loop gain only as the emitter diffusion resistance affects the open loop gain, assuming

$$r_E = \frac{KT}{q\ I_E} \cdot \tag{2-13}$$

This is evident from the third term of Eq. 2-10.

The ideal closed-loop gain expressed in Eq. 2-8 is not simply the ratio of two impedances, as in the case of base feedback with negligible source impedance. Consequently, emitter feedback does not lend itself well to producing operational functions such as integration, differentiation, summing, etc. Also from Eq. 2-8, the closed-loop gain must always be greater than one.

With respect to the amplifier configuration of Fig. 2-1, the common-mode rejection factor defined as the ratio of the common-mode (CM) input to the differential-mode (DM) input voltage that gives rise to the same output voltage is stated for differential and single-ended outputs as

$$CMR = \frac{A_{dd}}{A_{dc}} \qquad \text{(for differential output)} \tag{2-14}$$

$$CMR = \frac{(A_{dd} + A_{cd})}{(A_{cc} + A_{dc})} \qquad \text{(for single-ended output)} \tag{2-15}$$

where Table 2-I defines components.

A_{dd}	≡ Differential input to differential output gain
A_{cc}	≡ Common-mode input to common-mode output gain
A_{dc}	≡ Common-mode input to differential output gain
A_{cd}	≡ Differential input to common mode output gain

TABLE 2-I. AMPLIFIER GAIN COMPONENTS

Note that A_{dd} and A_{cc} are direct gain terms, and A_{cd} and A_{dc} are cross-coupled gain terms caused by circuit unbalances. If every parameter in the circuit was perfectly balanced, A_{cd} and A_{dc} would be zero. The following inequality is typically found in practice,

$$\frac{A_{dd}}{A_{dc}} > \frac{(A_{dd} + A_{cd})}{(A_{cc} + A_{dc})} \quad . \tag{2-16}$$

However, the amplifier specification being considered requires a high CMR factor for a single-ended output.

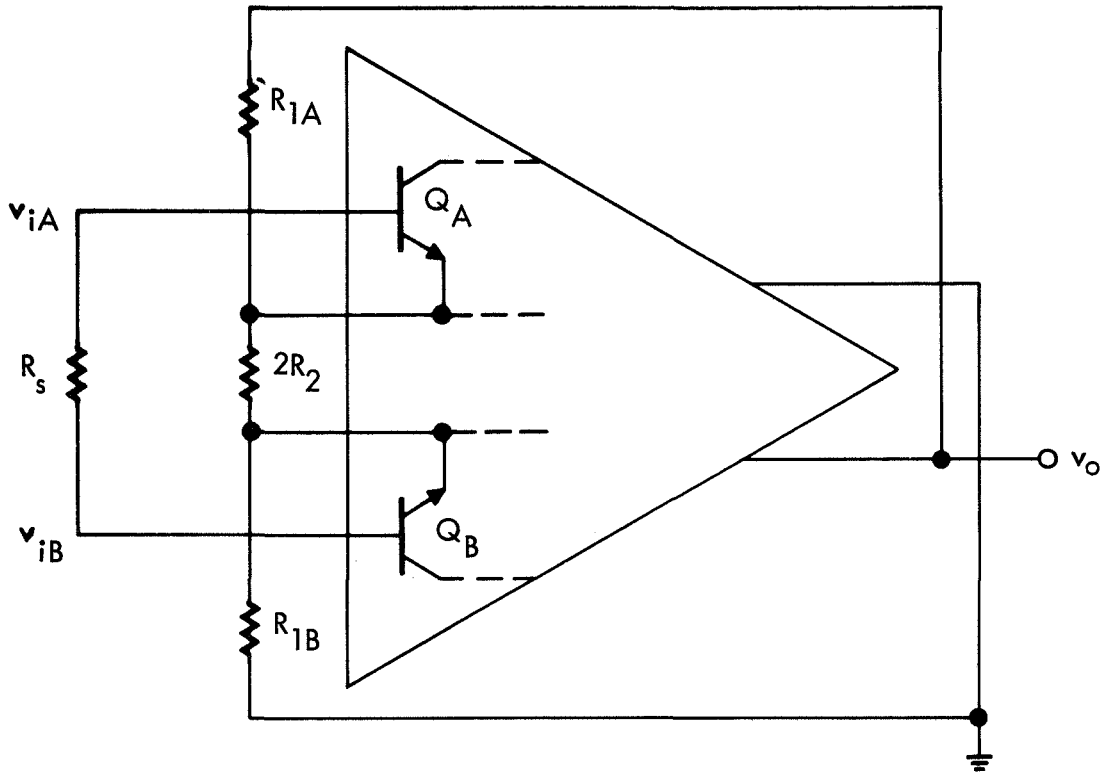

Fig. 2-3. Overall Emitter Feedback with One Output Grounded

The high value of CMR expressed in Eq. 2-14 can be realized for single-ended output with the feedback connection shown in Fig. 2-3. One output is grounded so that the differential and single-ended output voltages are identical. The high CMR factor expressed in Eq. 2-14 now applies.

In practice, the same CMR performance is obtained by only grounding the feedback resistor, as shown in Fig. 2-4, with S_1 in position one. Note, in this configuration, the effective open-loop gain is equal to one-half the differential gain of the open-loop amplifier.

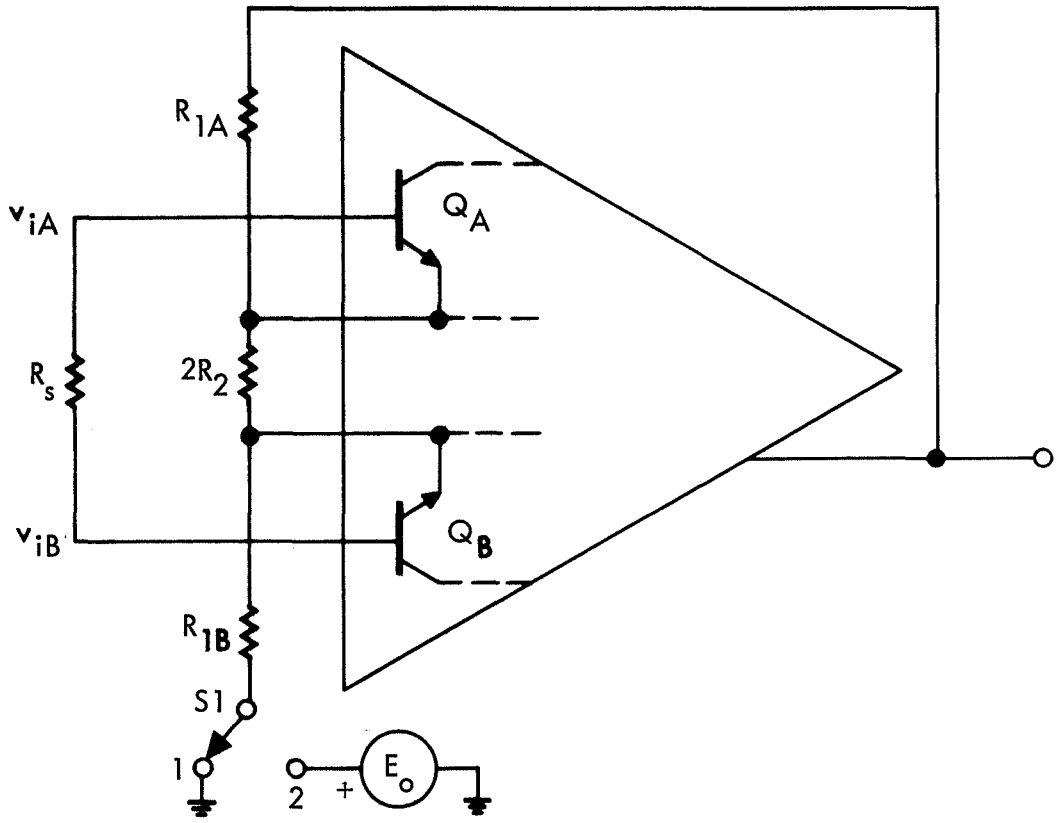

Fig. 2-4. Single-Ended Amplifier with Overall Emitter Feedback

If S_1 of Fig. 2-4 is in position two, the quiescent output voltage (zero differential input voltage) becomes E_o. This output offest is essentially independent of gain setting, thereby providing a convenient means for introducing the accurate +2.5 volt offset which is specified.

The effects of some important circuit unbalances will be examined by analyzing the circuit of Fig. 2-5. This simplified configuration does not include a common-mode circuit source into the input stage emitters and it assumes a zero source impedance. It is adequate for sake of discussion.

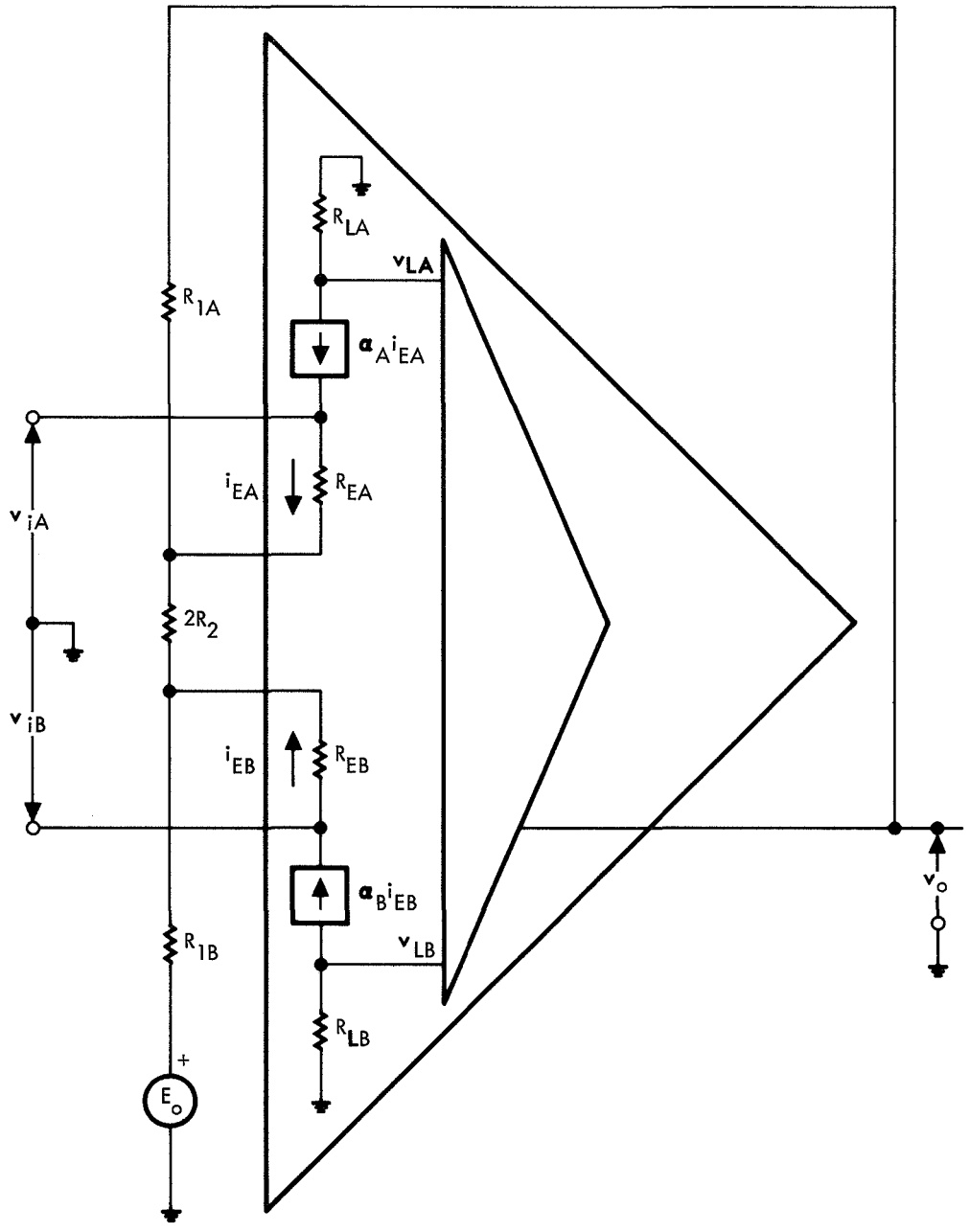

Figure 2-5. Overall Feedback Equivalent Circuit

The terms v_{iA} and v_{iB} include the external input signal in addition to the emitter-base voltages of the input stage.

Writing circuit equations for the configuration of Fig. 2-5 yields:

$$\begin{aligned} & v_o \left[\alpha_A R_{LA} \left(R_{1B}R_{EB} + 2R_2R_{1B} + 2R_2R_{EB}\right) - \alpha_B R_{LB} \left(R_{1B}R_{EA}\right) \right] \\ & = E_o \left[\alpha_B R_{LB} \left(R_{EA}R_{1A} + 2R_2R_{EA} + 2R_2R_{1A}\right) - \alpha_A R_{LA} \left(R_{1A}R_{EB}\right) \right] \\ & \quad + v_{iA} \left[\alpha_B R_{LB}R_{1A}R_{1B} + \alpha_A R_{LA} \left(R_{EB}R_{1B} + R_{EB}R_{1A} + R_{1A}R_{1B} \right.\right. \\ & \quad \left.\left. + 2R_2R_{EB} + 2R_2R_{1B}\right) \right] - v_{iB} \left[\alpha_A R_{LA}R_{1A}R_{1B} + \alpha_B R_{LB} \left(R_{EA}R_{1A} + R_{EA}R_{1B} \right.\right. \\ & \quad \left.\left. + R_{1B}R_{1A} + 2R_2R_{EA} + 2R_2R_{1A}\right) \right] . \end{aligned} \tag{2-17}$$

Note the similarity of the coefficients of v_o and E_o. If all symmetrical parameters are equal,

$$v_o = E_o \Big|_{v_{ia} = v_{ib}} , \tag{2-18}$$

which states that the output voltage is equal to the offset voltage, E_o, for zero differential input signals.

If the following parameters are assumed equal,

$$\alpha_A = \alpha_B = \alpha \tag{2-19}$$

$$R_{LA} = R_{LB} = R_L, \text{ and} \tag{2-20}$$

$$R_{EA} = R_{EB} = R_E, \tag{2-21}$$

Eq. 2-17 reduces to

$$v_o \left[2R_2 \ (R_{1B} + R_E) \right]$$

$$= E_o \left[2R_2 \ (R_{1A} + R_E) \right]$$

$$+ v_{iA} \left[R_{1A} \ (R_{1B} + R_E) + R_{1B} \ (R_{1A} + R_E) + 2R_2 \ (R_{1B} + R_E) \right]$$

$$- v_{iB} \left[R_{1A} \ (R_{1B} + R_E) + R_{1B} \ (R_{1A} + R_E) + 2R_2 \ (R_{1A} + R_E) \right] , \qquad (2\text{-}22)$$

which shows the effect of unbalances in R_{1A} and R_{1B}.

The following equations define the equivalent common-mode input signal, v_c, and the equivalent differential-mode input signal, v_d:

$$v_c \equiv \frac{v_{iA} + v_{iB}}{2} \qquad (2\text{-}23)$$

$$v_d \equiv \frac{v_{iA} - v_{iB}}{2} \qquad (2\text{-}24)$$

Eq. 2-23 and Eq. 2-24 yield

$$v_{iA} = v_c + v_d \qquad (2\text{-}25)$$

$$v_{iB} = v_c - v_d \qquad (2\text{-}26)$$

Substituting Eq. 2-25 and Eq. 2-26 into Eq. 2-22 yields

$$v_o \left[R_2 \ (R_{1B} + R_E) \right] = E_o \left[R_2 \ (R_{1A} + R_E) \right]$$

$$+ v_c \left[R_2 \ (R_{1B} - R_{1A}) \right]$$

$$+ v_d \left[R_{1A} \ (R_{1B} + R_E) + R_{1B} \ (R_{1A} + R_E) + R_2 \ (R_{1A} + R_{1B} + 2R_E) \right] \qquad (2\text{-}27)$$

For the case of $v_c = v_d = 0$

$$v_o = E_o \left[\frac{R_{1A} + R_E}{R_{1B} + R_E} \right] . \tag{2-28}$$

This indicates that E_o must be adjusted to give a precise amplifier output offset, for a fixed set of circuit parameters, i.e., typically $v_o \neq E_o$ because $R_{1A} \neq R_{1B}$. For the case of $v_c = E_o = 0$,

$$v_o = v_d \left[\frac{R_{1A} + R_2}{R_2} + \frac{R_{1B} + R_2}{R_2} \times \frac{R_{1A} + R_E}{R_{1B} + R_E} \right] . \tag{2-29}$$

If the second term of this equation is rewritten

$$\frac{R_{1A} + R_E}{R_2} \times \left[\frac{R_{1B} + R_2}{R_{1B} + R_E} \right] , \tag{2-30}$$

it can be seen that if $R_{1B} \gg R_2$ and $R_{1B} \gg R_E$, which is typically true, $\frac{v_o}{v_d}$ is primarily determined by R_{1A} and R_2, and has only a slight dependence on R_{1B}. For the case of $v_d = E_o = 0$,

$$v_o = v_c \left[R_{1B} - R_{1A} \right] \tag{2-31}$$

This equation shows that an output due to a common-mode input can be made equal to zero by setting $R_{1A} = R_{1B}$. However, in reality the case is considerably more complicated than this equation implies. For instance, the complete amplifier has many unbalances which degrade the CMR. The output can not be made zero, but can only be minimized. This is done by selecting the proper ratio of R_{1A} and R_{1B} to compensate for all of the other accumulated unbalances in the amplifier. Normally $R_{1A} \neq R_{1B}$ for optimum CMR.

In summary of Eq's. 2-28, 2-29, and 2-31, the resulting procedure for adjusting the amplifier is:

1. Adjust R_{1A} for precise gain (Eq. 2-29), then
2. Adjust R_{1B} for optimum CMR (Eq. 2-31), and then
3. Adjust E_o for precise amplifier output offset (Eq. 2-28).

Overall emitter feedback inherently provides high input impedance and low output impedance. From standard feedback analysis,[2] the input impedance is given as:

$$Z_{if} = Z_i \ (T + 1) \tag{2-32}$$

where $$T = \frac{\text{open loop gain}}{\text{closed loop gain}} \simeq \frac{A_T R_2}{R_1 + R_2} \tag{2-33}$$

$$Z_{if} \equiv \text{input impedance with overall feedback} \tag{2-34}$$

$$Z_i \equiv \text{input impedance without overall feedback} \tag{2-35}$$

Analysis of the equivalent circuit of Fig. 2-2 yields

$$Z_{if} = \frac{\partial v_i}{\partial i_i} = \beta R_E A_T \times \frac{R_2}{(R_1 + R_2)} , \tag{2-36}$$

which agrees with Eq. 2-32.

Also from standard feedback analysis, the output impedance is given as

$$Z_{of} = \frac{Z_o}{(T + 1)} \tag{2-37}$$

where $$Z_{of} \equiv \text{output impedance with overall feedback} \tag{2-38}$$

$$Z_o \equiv \text{output impedance without overall feedback} \tag{2-39}$$

---

[2] R. D. Middlebrook, "Design-Oriented Analysis of Feedback Amplifiers," National Electronics Conference, 19 October 1964

The predominant drift components of a differential amplifier are generated in the input stage and are primarily due to circuit parameter unbalances. The perfectly balanced circuit would develop zero drift (and give infinite common-mode rejection). The main contributors to input stage drift are differentials existing between the base-emitter voltages, current gains, and leakage currents of the input transistor pair. Each component is potentially non-linear with temperature; however, with proper design techniques, they can either be linearized or minimized.

The differential collector-base leakage currents flowing through the source resistance develop the most non-linear drift component, for it is proportional to the difference of two terms which increase exponentially with temperature. The silicon planar diffused transistors of the present-day integrated circuit exhibit room temperature leakage currents of about 0.1na. Assuming a doubling relationship with every $8^{o}C$ rise in temperature, this current increases to (0.1na) x 2^{7} at $+100^{o}C$, which is less than 15na. For the 350 ohm floating source configuration, the error at $+100^{o}C$ is $350 \left[(0.1 + \Delta I_{CBO}) \times 2^{7} - (0.1) \times 2^{7} \right]$ nv, where ΔI_{CBO} is the collector-base leakage current difference (in nanoamperes) of the two input transistors at room temperature. This error is normally less than 2 or 3μv and can be neglected. (Note, however, that if overall base feedback was used, this drift term would have made the amplifier an impossibility.)

The most significant source dependent drift term is due to differential base currents, caused by unequal transistor current gains which increase somewhat linearly with temperature. Assuming constant collector

currents, the base currents decrease with increasing temperature. The voltage error is directly proportional to the source resistance and is minimized by:

1. Designing the input stage to operate at very low collector current levels,
2. Maximizing the betas of the input transistor, and
3. Maximizing the beta match of the input transistors.

Given the 200na input current specification, together with minimum low temperature betas of 50, a maximum collector current is set at 10μa. Since the source is floating, a ± 10% input transistor beta match produces an equivalent input error of 14μv at low temperature. The linear portion of this temperature error component can be canceled. If 5 to 1 compensation is assumed, an uncompensated error of 2.8μv remains.

The base-emitter voltage is extremely temperature sensitive, having a temperature coefficient of approximately -2.2mv/^{o}C. Assuming an identical pair of transistors, a 0.001^{o}C temperature difference will produce a 2μv voltage differential. Low level operation of the input stage enhances the drift performance at this point. Take, for instance, a transistor pair A operating at 10μa collector current and 3 volts collector-emitter voltage. A thermal resistance of 500^{o}C/W (for illustration) leads to a 0.015^{o}C temperature increase. In contrast, a transistor pair B operating at 100μa and 5 volts raises the temperature 0.25^{o}C. The probability of maintaining exactly equal temperatures between transistors is much higher for pair A than for pair B. The thermal imtimacy provided by the entire integrated circuit lends itself to minimum drift performance. A high degree of compensation results from insuring the

transistor input pair and the drift-offset control circuit experience the same temperature.

The differential base-emitter voltages of the input transistors is the dominant drift term. It can be shown that this component is highly linear with temperature if the collector currents of the input transistor pair are held constant.[3] It has also been found that maximum temperature tracking is obtained by selecting input transistors with the closest V_{BE} match.[4]

It is the object of this design to hold the collector currents of the input stage constant and equal. This results in a linear temperature drift term which, together with the other accumulated drift terms, can be effectively compensated.

Two basic approaches were considered for designing this minimum drift, direct coupled, differential amplifier.

1. Maximize the linearity of the inherent temperature drift and add a direct compensating temperature dependent linear voltage to cancel the inherent drift, and/or

2. Minimize the inherent temperature drift by a "self compensation" technique.

Hoffait and Thornton[3] describe the second technique in which passive circuit component unbalances are used to compensate for differences in transistor parameters. This approach yields equivalent input drifts less than $0.1\mu v/^{o}C$, but simultaneously deteriorates the common-mode rejection because of the intentional circuit unbalances. This problem is acknowledged in their paper "Limitations of Transistor DC Amplifiers," and a suggested

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[3] A. H. Hoffait and R. D. Thornton, "Limitations of Transistor DC Amplifiers," Proc. IEEE (February 1964)

[4] A. Tuszynski, "Correlation of Base-Emitter Voltage and Temperature Coefficient," Solid State Design 3, 32-35 (July 1962)

solution is to provide a floating power supply for the input stage.

Middlebrook describes the use of the first technique in "Differential Amplifier with Regulator Achieves High Stability, Low Drift."[5] This approach is considered more practical because of the relative ease in obtaining high common-mode rejection figures. The drift performance of this direct compensation technique, as demonstrated in the laboratory, also yields equivalent input drifts less than $0.1\mu v/^{o}C$.

With reference to the block diagram of Fig. 2-6, direct drift and offset compensation is accomplished by supplying currents (which have a linear temperature dependent component) from the drift-offset control circuit to flow through the feedback resistors. This adds a linear temperature-dependent voltage in series with the input signal to cancel the accumulated inherent amplifier drift. The effectiveness of this drift compensation is directly related to the linearity of the inherent and compensating drift components.

Currents I_{Ao} and I_{Bo} control the output voltage according to

$$v_o = (I_{Ao} - I_{Bo})\, R_1 + (v_A - v_B)\, \frac{R_1 + R_2}{R_2}\,, \tag{2-40}$$

assuming $R_{1A} = R_{1B} = R_1$. The $(v_A - v_B)$ term represents an equivalent differential input term. The drift-offset control circuit is adjusted such that

$$(I_{Ao} - I_{Bo})\, R_1 = (v_B - v_A)\, \frac{R_1 + R_2}{R_2} \quad \text{(zero offset)} \tag{2-41}$$

[5] R. D. Middlebrook, "Differential Amplifier with Regulator Achieves High Stability, Low Drift," Electronics (July 1964)

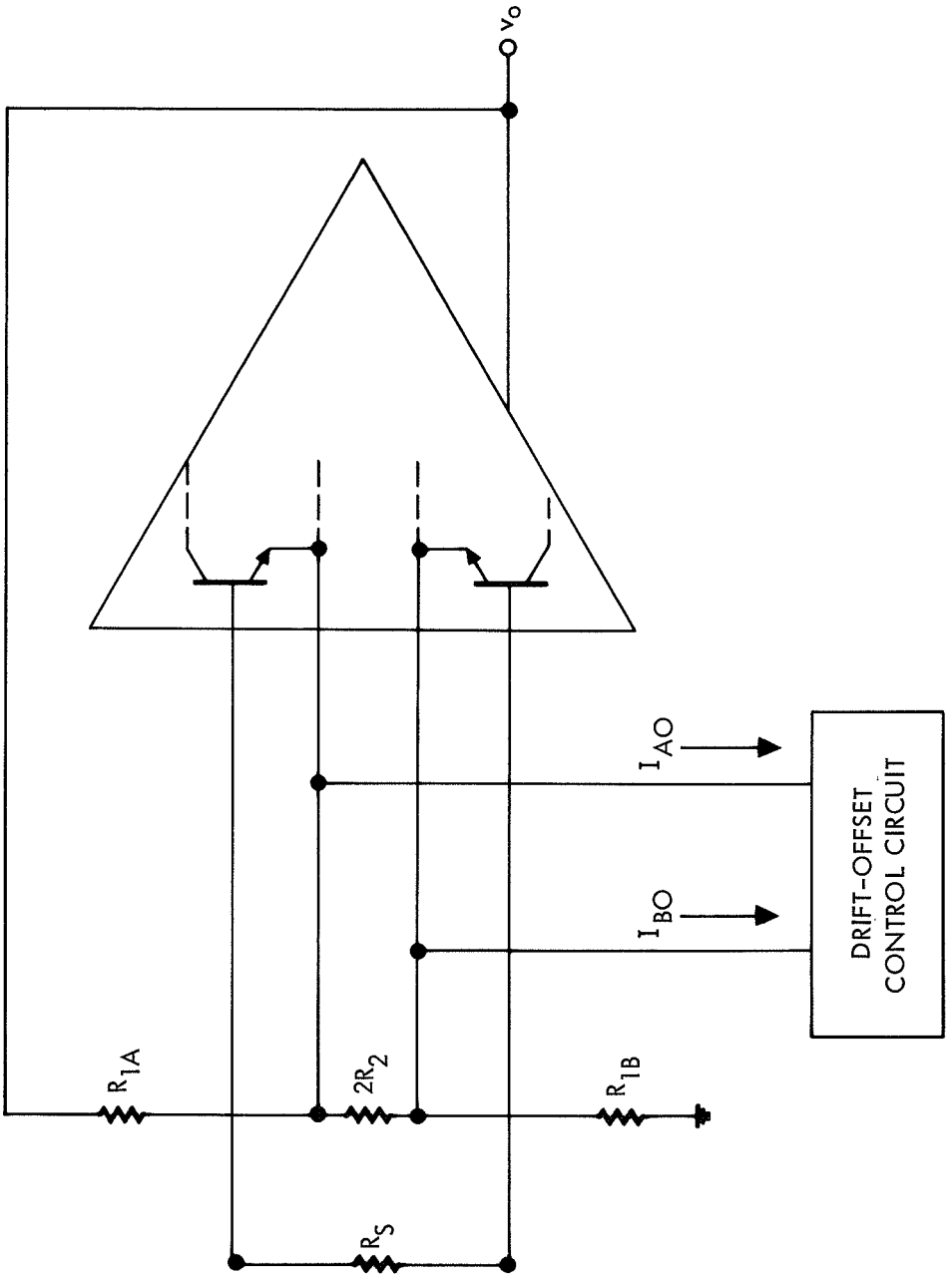


Fig. 2-6. Direct Compensation Technique

and $$\left[\frac{\partial}{\partial T}\,(I_{Ao} - I_{Bo})\right] R_1 = \left[\frac{\partial}{\partial T}\,(v_B - v_A)\right] \frac{R_1 + R_2}{R_2} \quad \text{(zero temperature drift)} \tag{2-42}$$

For this case, the drift-offset compensation can be maintained for different gain settings if R_2 is held constant and R_1 is changed.

For the case of $R_{1A} \neq R_{1B}$, the first term of Eq. 2-40 becomes

$$I_{Ao}R_{1A} - I_{Bo}R_{1B}\left[\frac{G_{1A} + G_{EA}}{G_{1B} + G_{EB}}\right], \tag{2-43}$$

which shows that the degree of drift offset compensation is a function of the balance of R_{1A} and R_{1B}, etc.

Three techniques are employed in this amplifier to insure high common-mode rejection.

1. Attention is given to obtain well matched resistors initially. CMR is maximized for a given differential closed loop gain by minimizing the cross-coupling term A_{dc}, Eq. 2-14. If every symmetrical circuit parameter was balanced, the A_{dc} term would be zero. Common-mode changes in bias levels are converted to differential signals by the circuit unbalances, which in turn are differentially amplified. Consequently, unbalances near the input of the amplifier degrade the CMR more severely than those near the output. For this reason, a resistor trimming capability is included for the collector load resistors of the input stage. In general, good matching is obtained in an unadjusted pair of thin film resistors deposited in close proximity of one another. It is therefore expected that a properly designed integrated circuit inherently lends itself to high common-mode rejection figures.

2. Common-mode negative feedback is incorporated.

The first technique of increasing the CMR is to maximize the balance of component values which are exposed to common-mode bias variations. The second technique is to minimize the common-mode bias variations by a high gain negative feedback loop. In principle, if the bias levels were absolutely stable with changing common-mode input voltages, no differential terms would be generated by the unbalances, and the CMR would be infinite. The effects of circuit unbalances are consequently decreased by the factor that the common-mode bias levels are stabilized, the value of T for the common-mode feedback loop, Eq. 2-33. For instance, if two resistors are unbalanced by $\pm$ 1%, and these resistors are included in a common-mode feedback loop with T = 40 dB, the effective resistor unbalance is reduced to $\pm$ 0.01%.

The common-mode input impedance is also increased by the negative feedback, as given in Eq. 2-32. This allows high CMR to be maintained in the environment of an unbalanced source configuration. The common-mode input impedance needed to insure a stated CMR figure in the presence of a ΔR_s maximum source impedance unbalance is given as

$$Z_{in\text{-}cm} > (\Delta R_s) \times (CMR) \qquad (2\text{-}44)$$

One difficulty in using single-ended overall emitter feedback is the input stage bias level dependence on the common-mode input voltage and output voltage swing. For instance, considering the design values of this particular design, the extreme conditions formed by a $\pm$ 1 volt common-mode input and a 0 to +5 volt output swing causes the currents in the feedback

resistors to change more than 200μA. Yet, the emitter currents of the input transistors must be stabilized at 10μA. A high common-mode loop gain also provides this stability.

High loop gain is obtained by incorporating two circuit features; a bootstrapping circuit and a common-mode voltage regulator amplifier. Figure 2-7 shows a basic schematic of the common-mode feedback loop which includes the bootstrapping circuit and the regulating amplifier. R_{4A} and R_{4B} are the collector load resistors of the input stage. The CM voltage across these resistors is held relatively constant and equal to the voltage across R_5. The diode D maintains the voltages across R_5 and R_{4A}-R_{4B} approximately constant with temperature. The second-stage emitter voltage, v_{E2}, is monitored and compared with a reference. This comparison is amplified by $\frac{1}{R_C}$ and converted to a current to supply the input stage emitters.

A common-mode equivalent circuit is shown in Figure 2-8. From the analysis of this model, the effective common-mode load resistance of the input stage is found to be approximately,

$$R_4' \simeq \frac{R_{4A} + R_{4B}}{2} \times \frac{R_3}{R_5} \tag{2-45}$$

The bootstrapping circuit therefore provides an increase in common-mode loop gain of approximately

$$\frac{R_3}{R_5} . \tag{2-46}$$

The value of T for the common-mode feedback loop becomes

$$T \simeq \frac{R_7}{R_6 + R_7} \times \frac{1}{R_C} \times R_4 \times \frac{R_3}{R_5} . \tag{2-47}$$

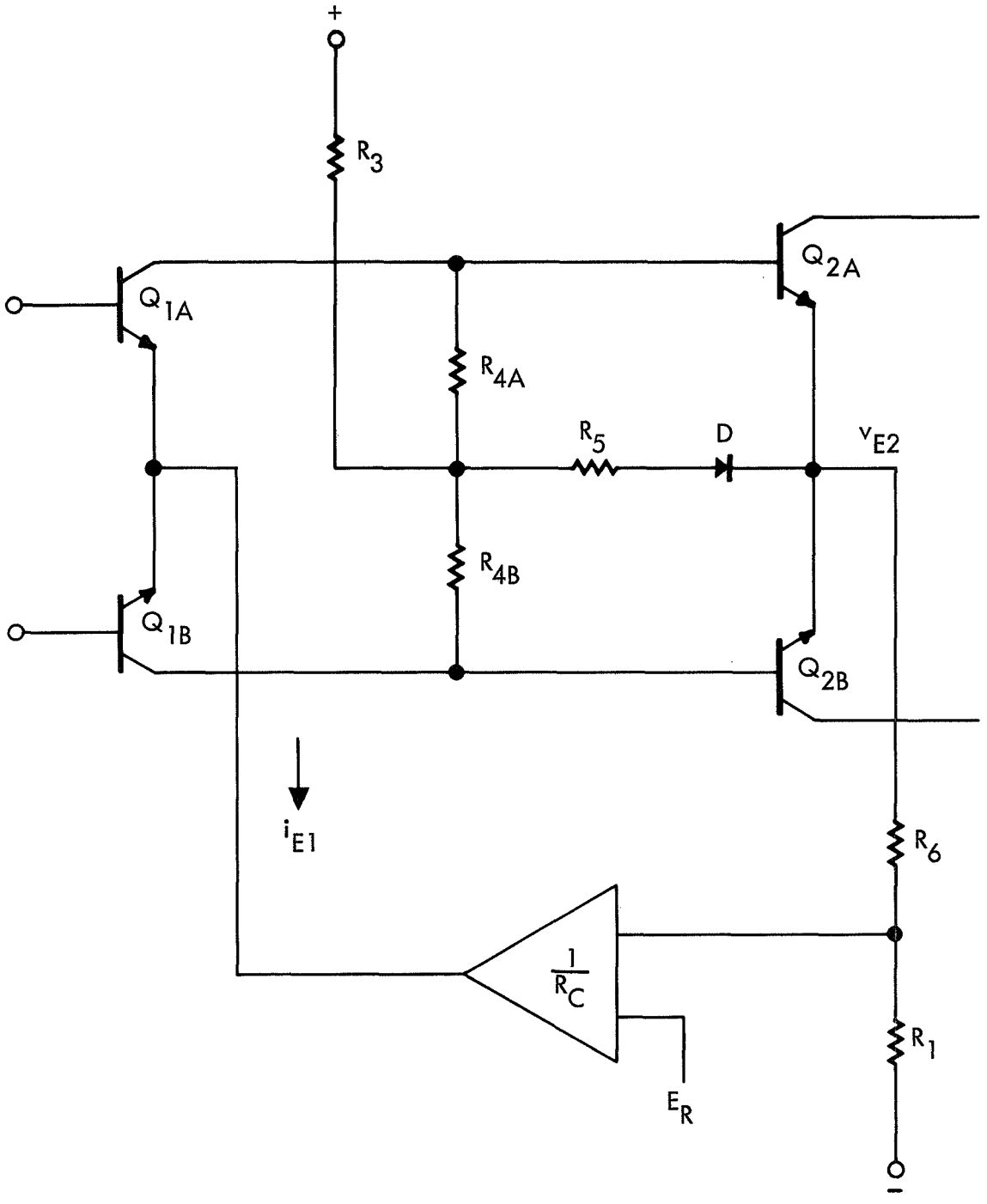


Figure 2-7. Basic Schematic of Common-Mode Feedback Loop

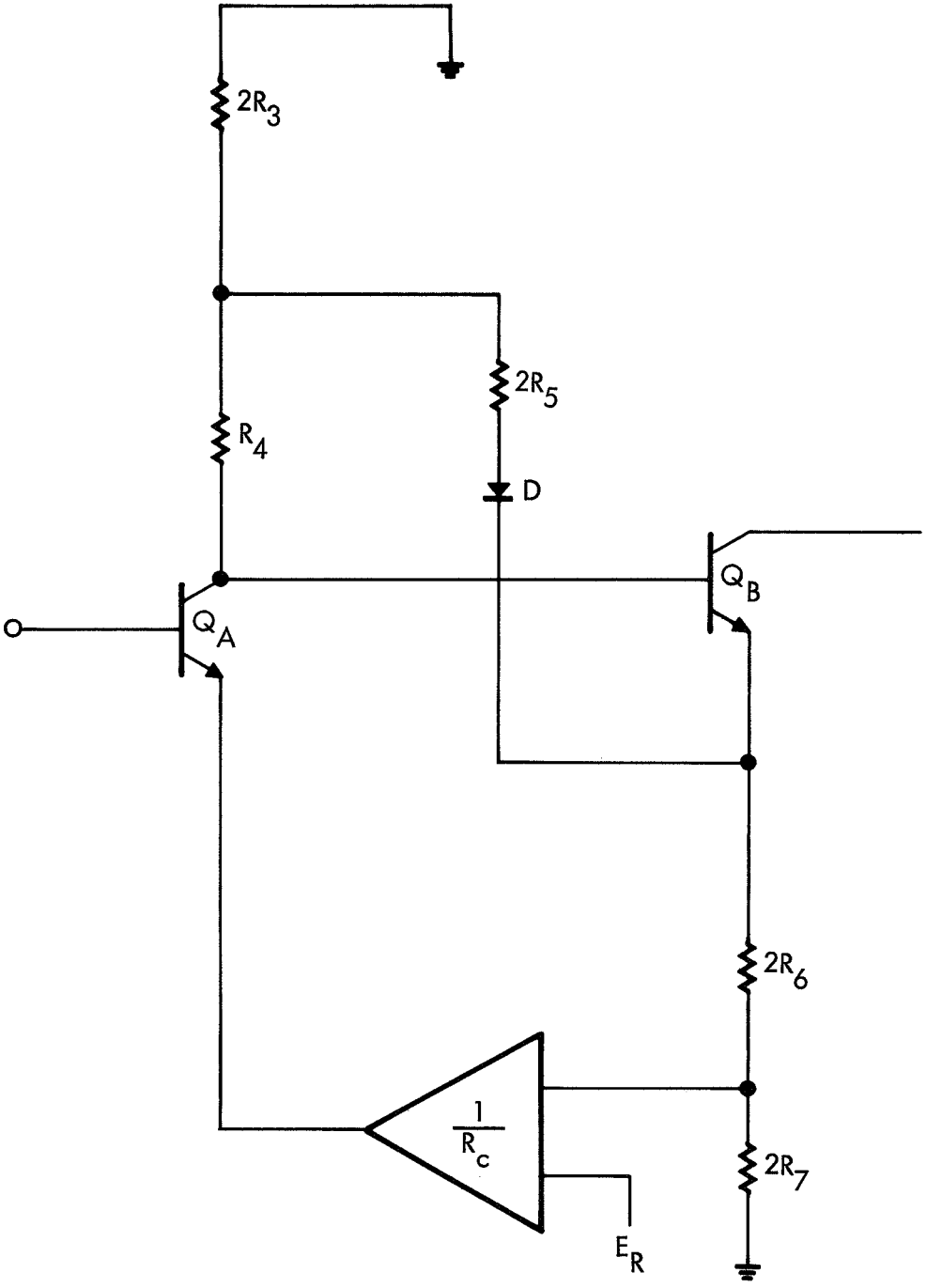


Figure 2-8. Common-Mode Equivalent Circuit of Common-Mode Feedback Loop

3. The overall feedback resistors are trimmed.

Eq. 2-31 shows that for a perfectly balanced amplifier, the output component due to a common-mode input voltage can be made zero by setting $R_{1A} = R_{1B}$. However, in the general case for an amplifier which is not perfectly balanced, optimum CMR figures are obtained with $R_{1A} \neq R_{1B}$. Since R_{1A} primarily determines the gain, R_{1B} is trimmed to yield optimum CMR. This adjustment tends to compensate for the effects of accumulated circuit unbalances.

2.1.3 Drift-Offset Compensation Circuit

Figure 2-9(a and b) shows the basic circuit of the drift control and the offset control, respectively. Each circuit supplies current to the amplifier overall feedback resistors to compensate for the inherent amplifier drift and offset.

The drift control circuit operates as follows. If the collector currents of Q_A and Q_B, together with the betas of Q_A and Q_B, are assumed to be approximately equal, then the base currents will be equal. For equal base currents, the current through R_A will be exactly equal to the output collector current of Q_A over the entire temperature range. If the collector current of Q_B is approximately constant with temperature, the change of V_{BE} of Q_B will be highly linear with temperature. The current through R_A, which is equal to the output current, will therefore be a highly linear function of temperature. The derivative of current with respect to temperature will be negative and inversely proportional to R_A.

The offset control circuit operates as follows. The connection of Q_D and Q_C is a 100% feedback loop, such that the voltage across R_C is stabilized with respect to temperature if R_D/R_E is equal to the α of Q_D. (The voltage gain of Q_D, R_E, and R_D is unity.) As argued in the above paragraph, the

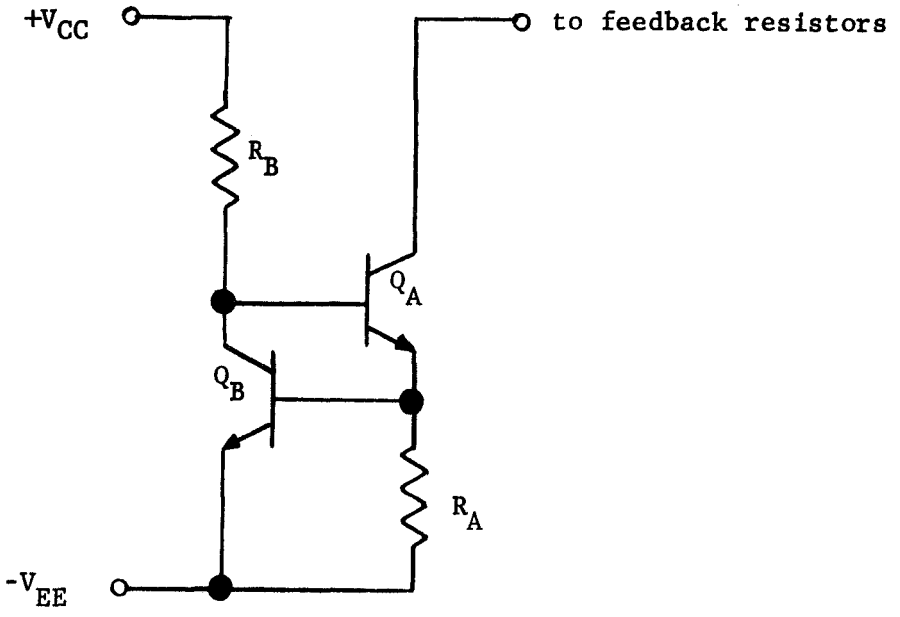


Figure 2-9(a). Drift Control Circuit

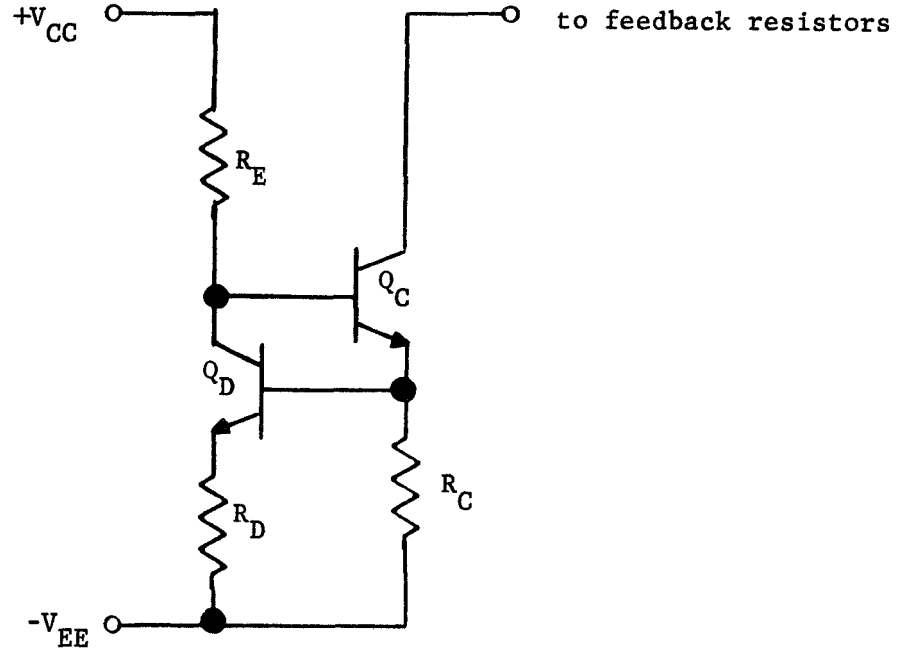


Figure 2-9(b). Offset Control Circuit

output collector current of Q_C is equal to the current through R_C; therefore, the output current is constant with temperature and inversely proporational to R_C.

2.2 CIRCUIT DESCRIPTION

Figure 2-10 shows the complete schematic which includes the basic amplifier and the drift-offset compensation circuit. The basic amplifier is described as follows.

Q_1 and Q_2 are the common-emitter differential input stage. Resistors R_1 and R_2 are available to supply base current if the source impedance is floating. Resistor R_7 supplies current from the positive supply into the feedback resistors, R_{37}, R_{38}, R_{39}, and R_{40}. This current is needed when the output voltage goes negative or the common-mode input voltage goes positive. Resistors R_{12} and R_{13} are the collector load resistors of the input stage. Capacitors C_1 and C_2 provide the dominant pole in the common-mode closed feedback loop and provide a 10 kHz pole in the differential loop which exactly cancels the 10 kHz zero introduced by the feedback network.

Resistors R_{11}, R_{12}, R_{13}, and R_{15}, in addition to transistors Q_7, Q_8, Q_{12}, Q_{13}, and diodes Q_{10} and Q_{11}, form a bootstrapping network which increases the common-mode loop gain. Transistors Q_7 and Q_8 are emitter followers preceding the second common-emitter differential gain stage, Q_{12} and Q_{13}. Diode Q_9 and resistors R_{16} and R_{17} establish the emitter currents of Q_7 and Q_8. Resistors R_{18} and R_{19} are the collector load resistors of the second gain stage. Transistors Q_{14} and Q_{15} are current generators which, with R_{20} and R_{23}, form differential dc level shifters. Emitter followers Q_{17} and Q_{18} drive the third and last gain stage, Q_{19} and Q_{20}. R_{31} is the collector load resistor of Q_{20}. Emitter followers Q_{21} and Q_{22} provide output current drive

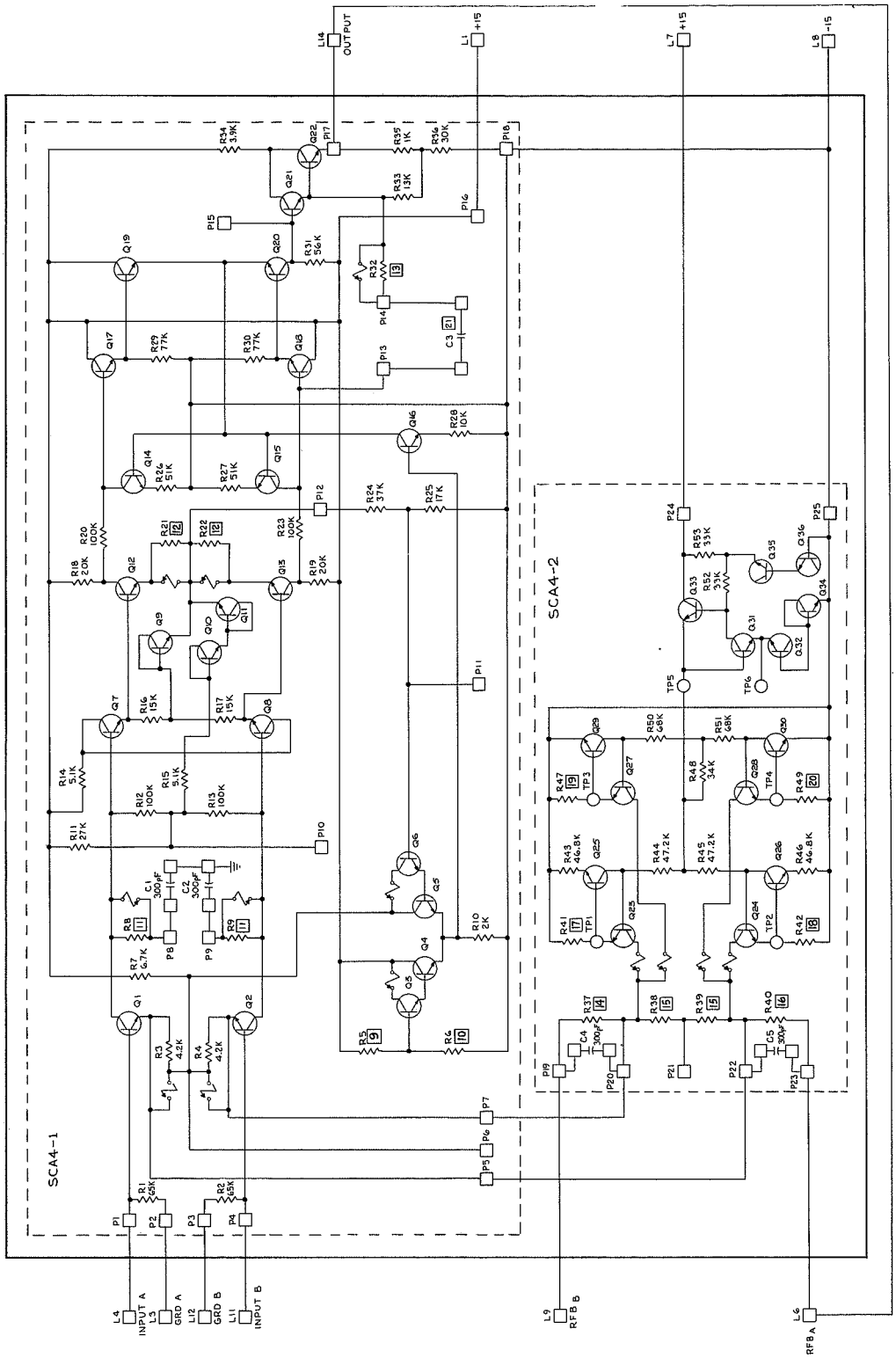


Figure 2-10. Signal Conditioning Amplifier Schematic

into a load. Current generator Q_{16} delivers common-mode emitter current into the third differential gain stage.

Transistors Q_3, Q_4, Q_5, and Q_6 form the common-mode feedback amplifier which stabilizes the common-mode voltage across R_{12} and R_{13} by regulating the voltage at the emitters of Q_{12} and Q_{13}. This feedback loop maintains the common-mode collector currents of Q_1 and Q_2 stable at 10μA.

The drift-offset compensation circuit and feedback resistors are found on the lower half of Figure 2-10. Transistor pairs Q_{27}/Q_{29} and Q_{28}/Q_{30} form the drift control circuits. R_{47} and R_{49} are adjusted for drift compensation. Transistor pairs Q_{23}/Q_{25} and Q_{24}/Q_{26} form the offset control circuit. R_{43} and R_{46} are adjusted for offset compensation. Transistors Q_{31}, Q_{32}, Q_{33}, Q_{34}, Q_{35}, and Q_{36} form a voltage regulator that stabilizes the supply voltage of the drift and offset circuits. Q_{35} and Q_{36} are used as zener diode pre-regulators. The output voltage is established by diodes Q_{32} and Q_{34}. Transistor Q_{31} compares the output with this diode reference to control the series regulating transistor Q_{33}.

Capacitors C_4 and C_5 across the feedback resistor establish the closed loop 6 dB per octave pole at 10 kHz. Capacitor C_3 is multiplied by the Miller effect to provide the dominant control pole in the differential mode loop.

Figure 2-11 shows the resistor adjustments available on the feedback resistors and drift-offset compensation circuit.

2.3 INTEGRATED CIRCUIT DESCRIPTION

The complete circuit is divided into the following sections:

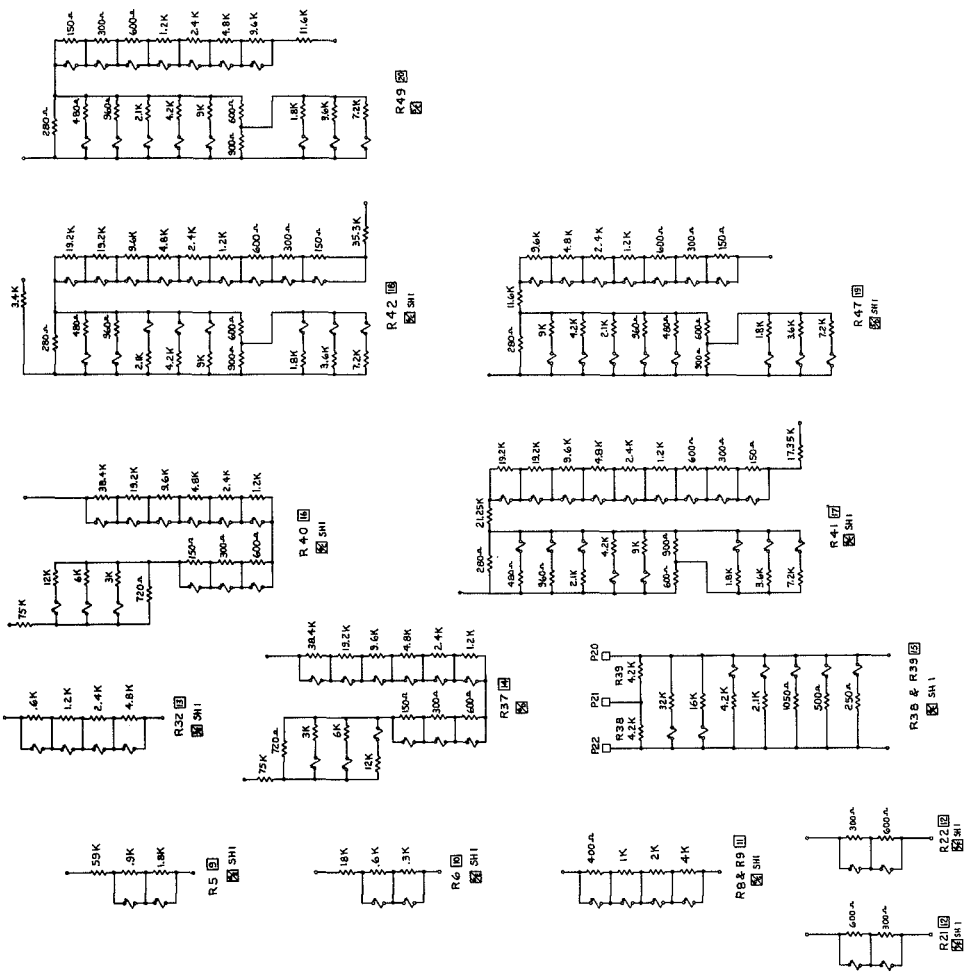


Figure 2-11. Signal Conditioning Amplifier Resistors

1. SCA41 (Basic Amplifier)

2. SCA42 (Drift Offset Compensation Circuit with Feedback Resistors)

3. Capacitors

The active component circuitry is divided into two dice for the following reasons.

1. Functionally, the Basic Amplifier will operate independently as an open loop amplifier, allowing a broad application of this die. The addition of the second active component die provides precise control of the drift and offset, and converts the open loop amplifier into a closed loop, precise gain configuration. (The MOS stabilization capacitors form the third die.) In summary, this die division was chosen for functional reasons.

2. The overall feedback resistors are on the same die as the drift-offset control circuit because of thermal tracking requirements of the cermet thin film resistors. For instance, the amplifier output thermal drift is controlled by the ratio of two resistors; one found in the drift-offset control circuit, the other in the feedback resistor network. It is important that this ratio is relatively constant with temperature, to avoid creating nonlinearities in the drift performance.

3. All of the adjustments are performed on the drift-offset, feedback resistor die. Therefore, if the die is damaged during the adjustment procedure, it can be replaced without having to discard the amplifier and capacitor die.

4. The surface area and the number of active devices required by each circuit lend themselves to this die division.

5. This division also allows a minimum number of inter-die connections.

The basic amplifier assembly drawing of Figure 2-12 shows the 1.2 megohms of resistors and 22 buried layer epitaxial transistors on the 95 x 115 mil die. Figure 2-13 is a photograph of a SCA41 wafer. Figures 2-14 and 2-15 show the MCD4 substrate and a lateral view of the transistor geometry, respectively. Figures 2-16 through 2-23 illustrate each mask separately. The drift-offset compensation circuit with feedback resistors, SCA42, is shown in Figure 2-24. All of the adjustments are performed on this die. The MCD4 is used also for this die.

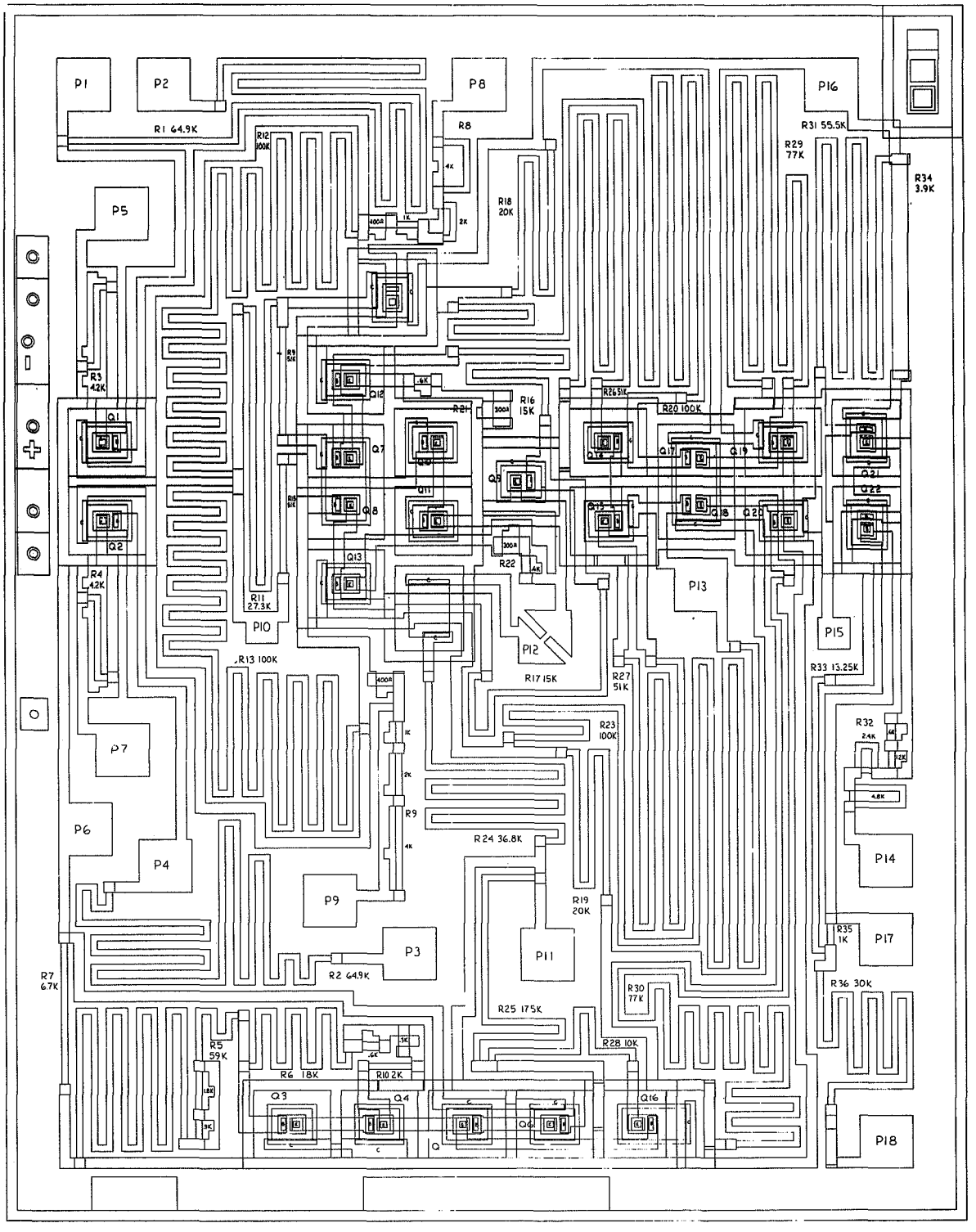


Figure 2-12. SCA41 Assembly Drawing

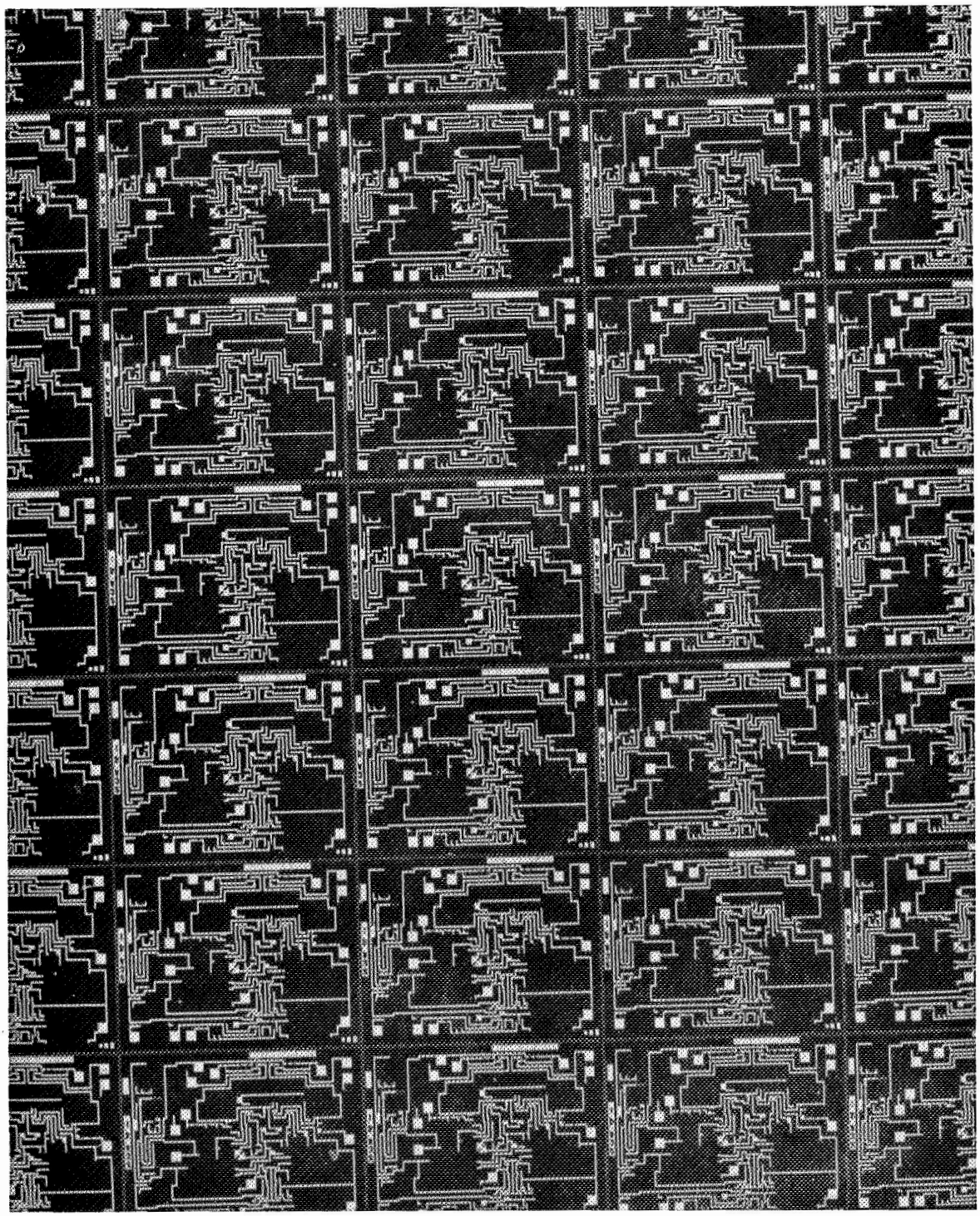


Figure 2-13. Photograph of SCA41 Wafer

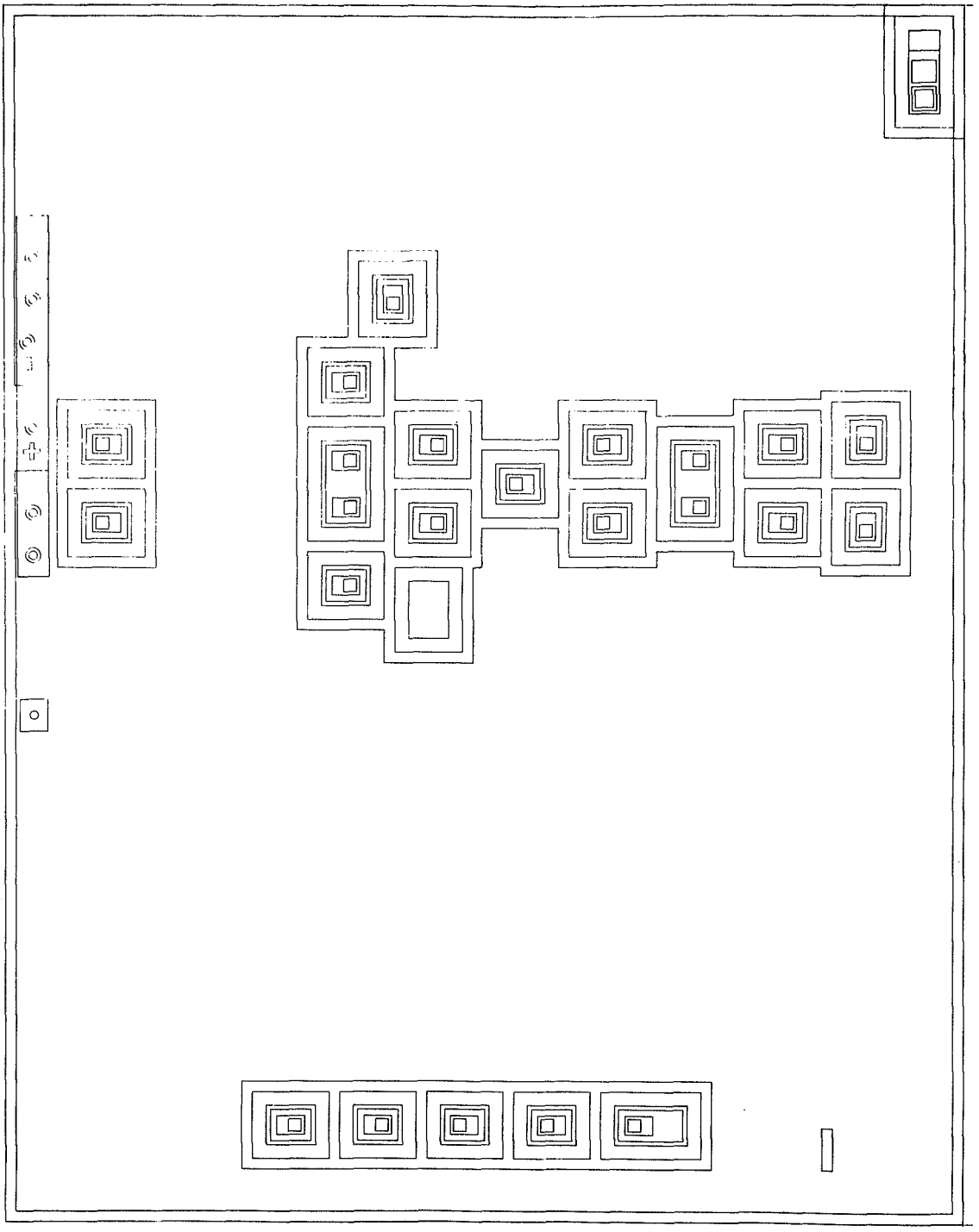
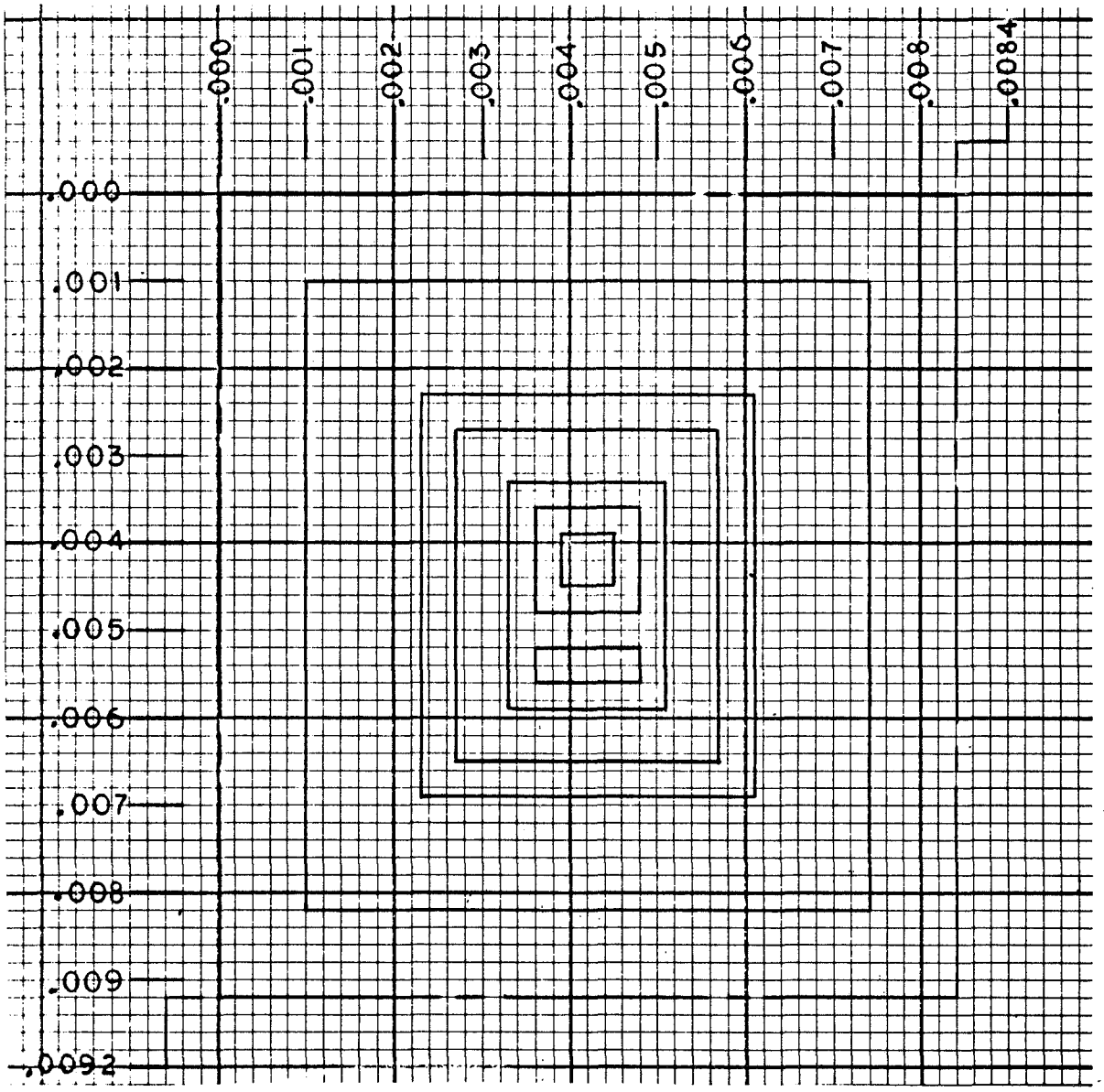


Figure 2-14. Multi-Circuit Die Common Substrate (MCD4) Drawing



Scale 500:1

Figure 2-15. MCD4 Transistor Structure

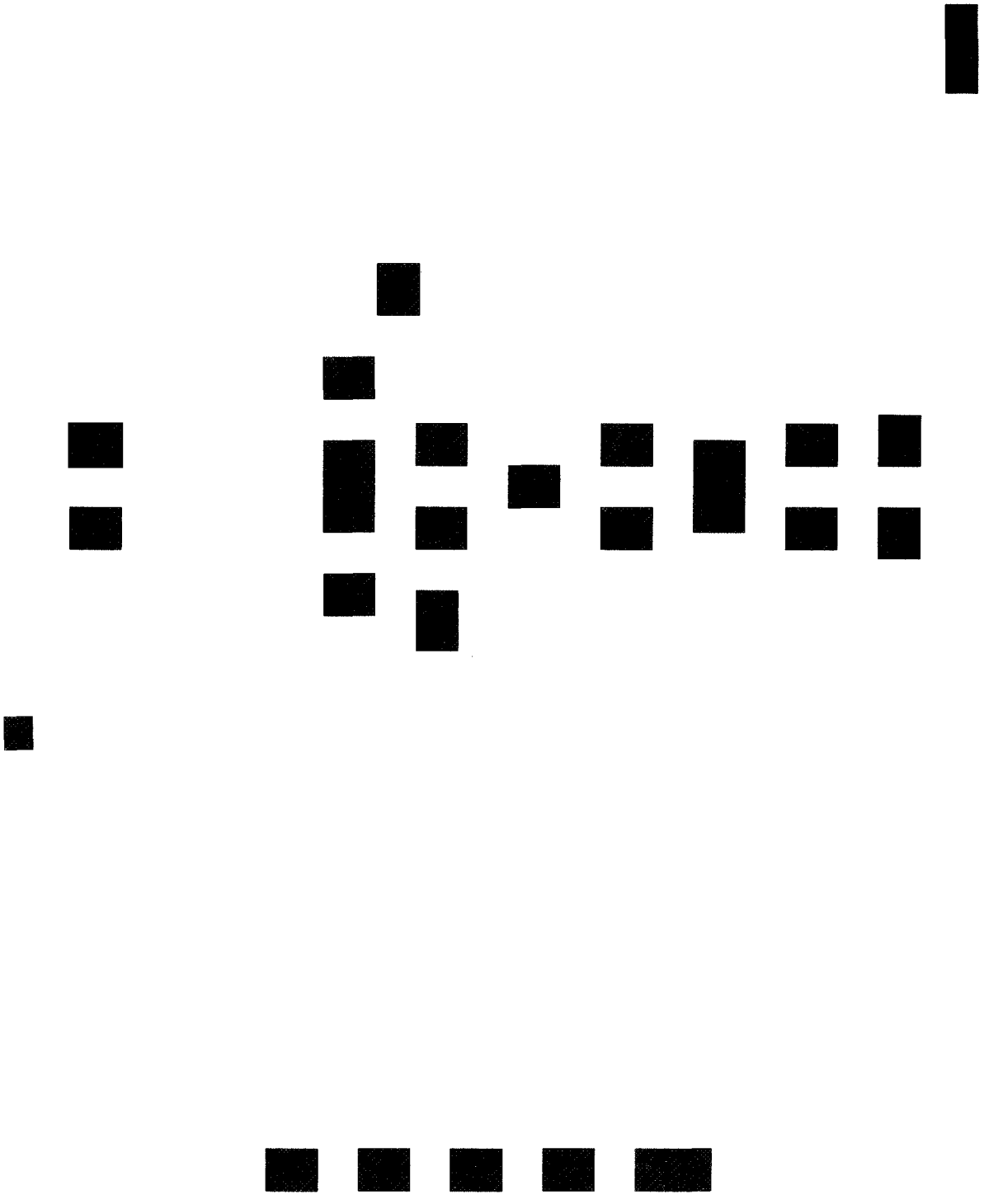


Figure 2-16. Buried Layer

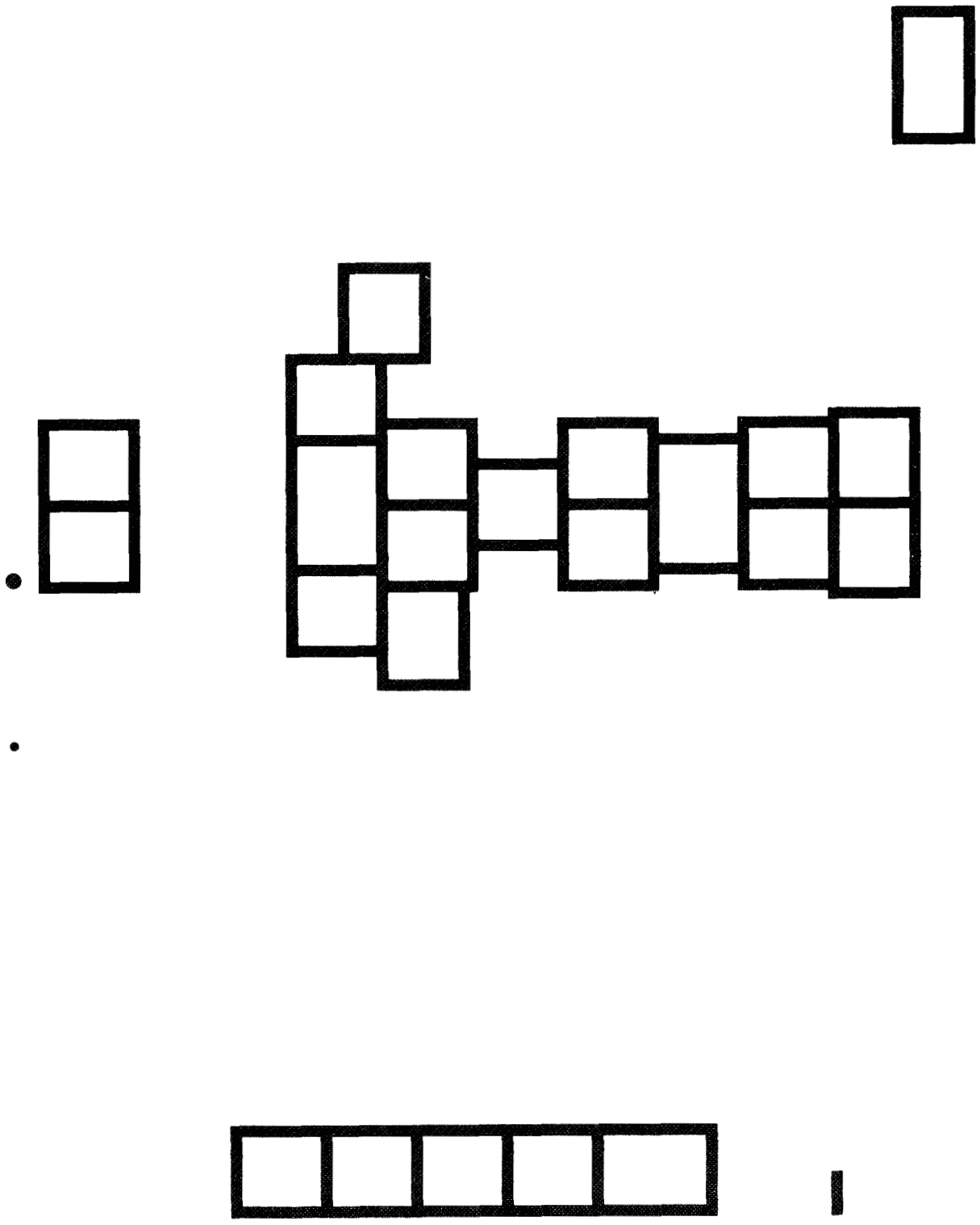


Figure 2-17. Isolation Gate

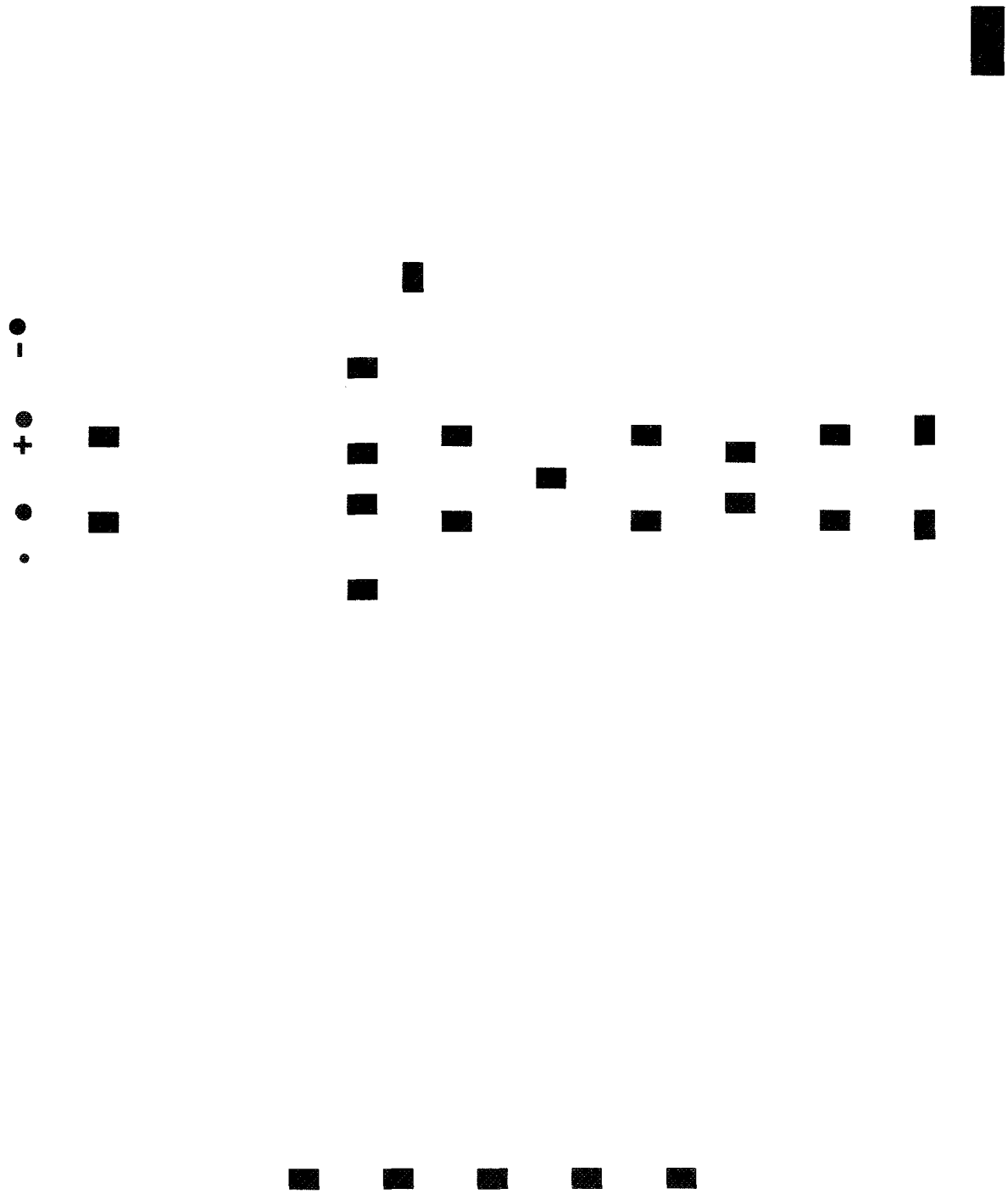


Figure 2-18. Base

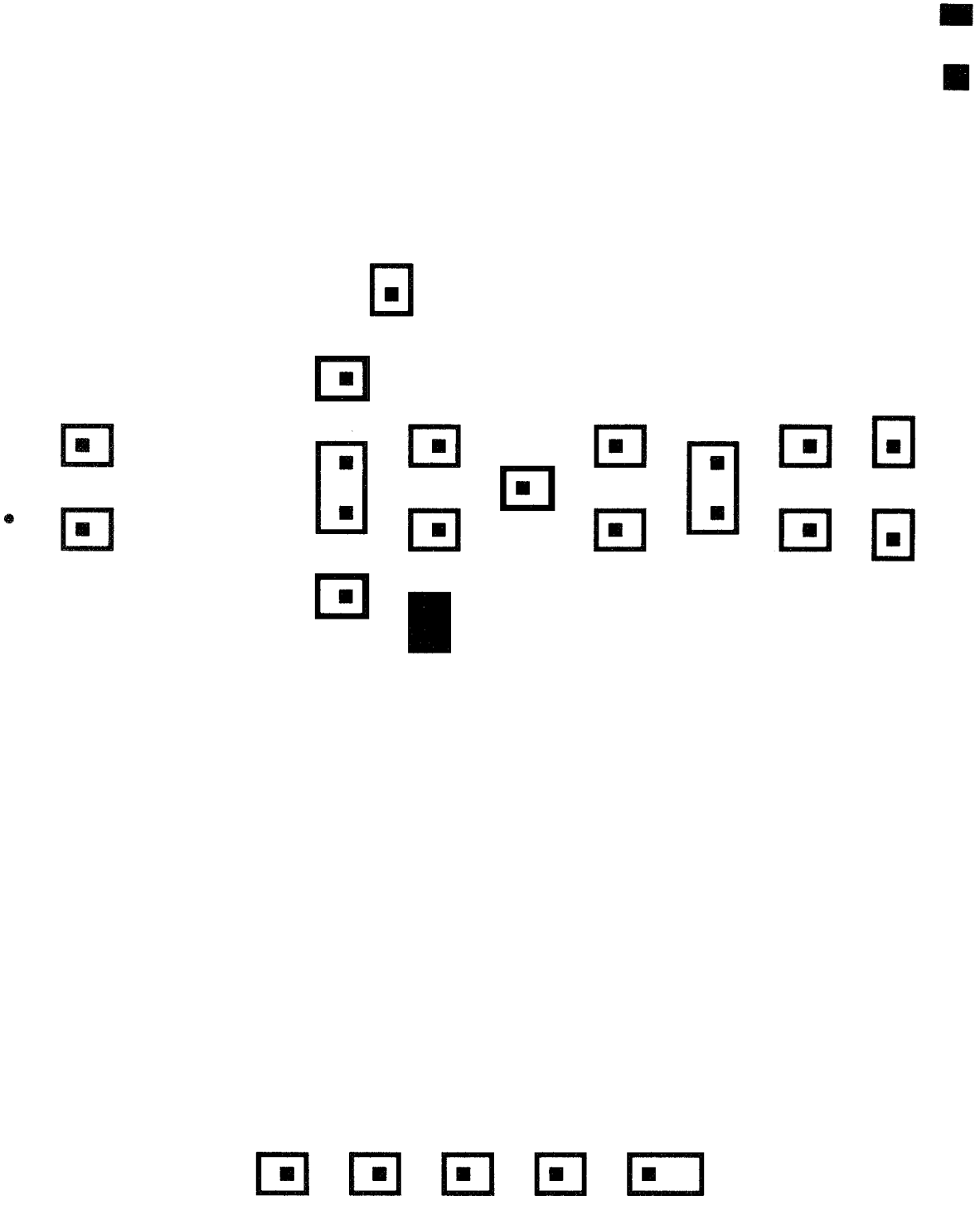


Figure 2-19. Emitter

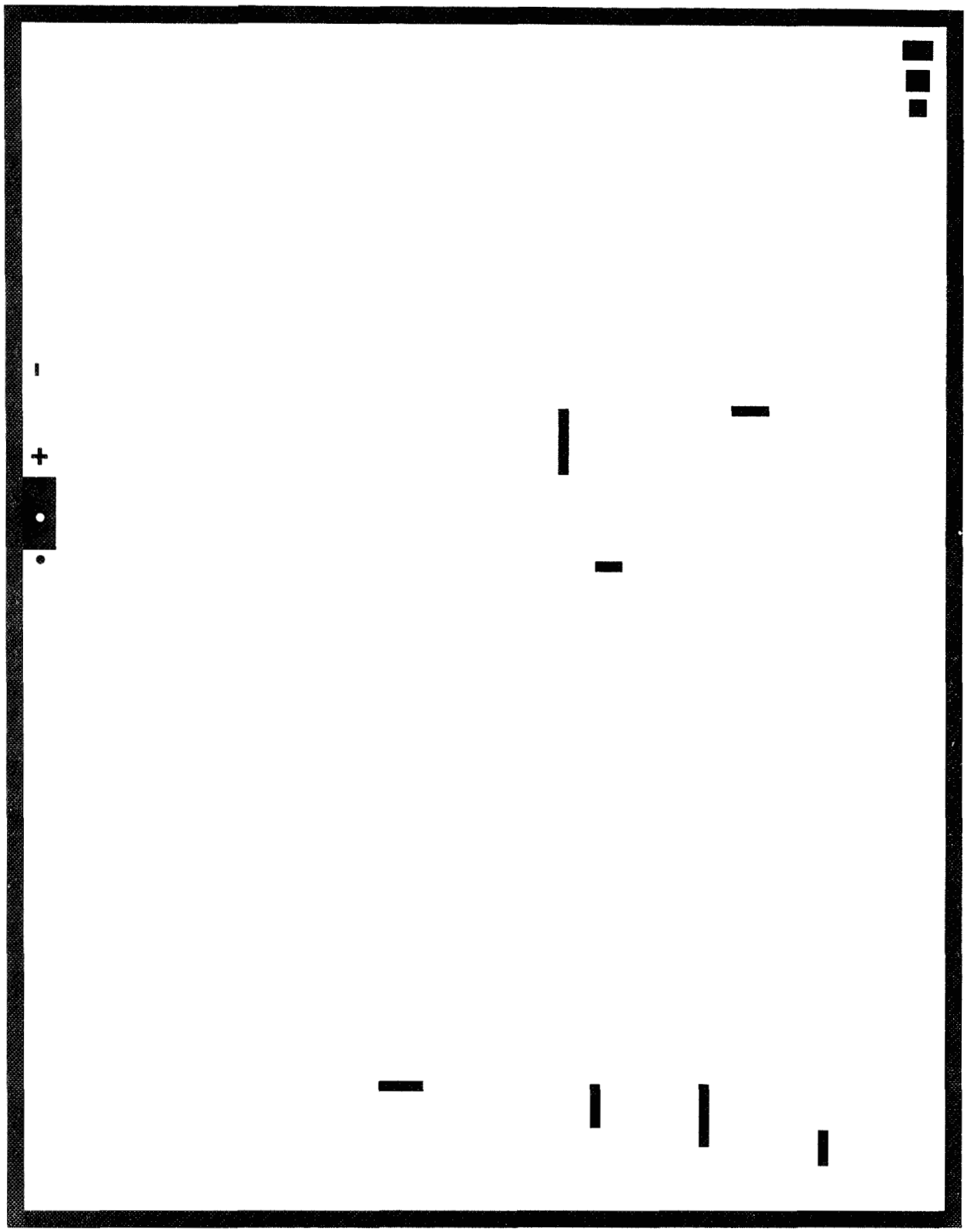


Figure 2-20. Test Transistor Contact

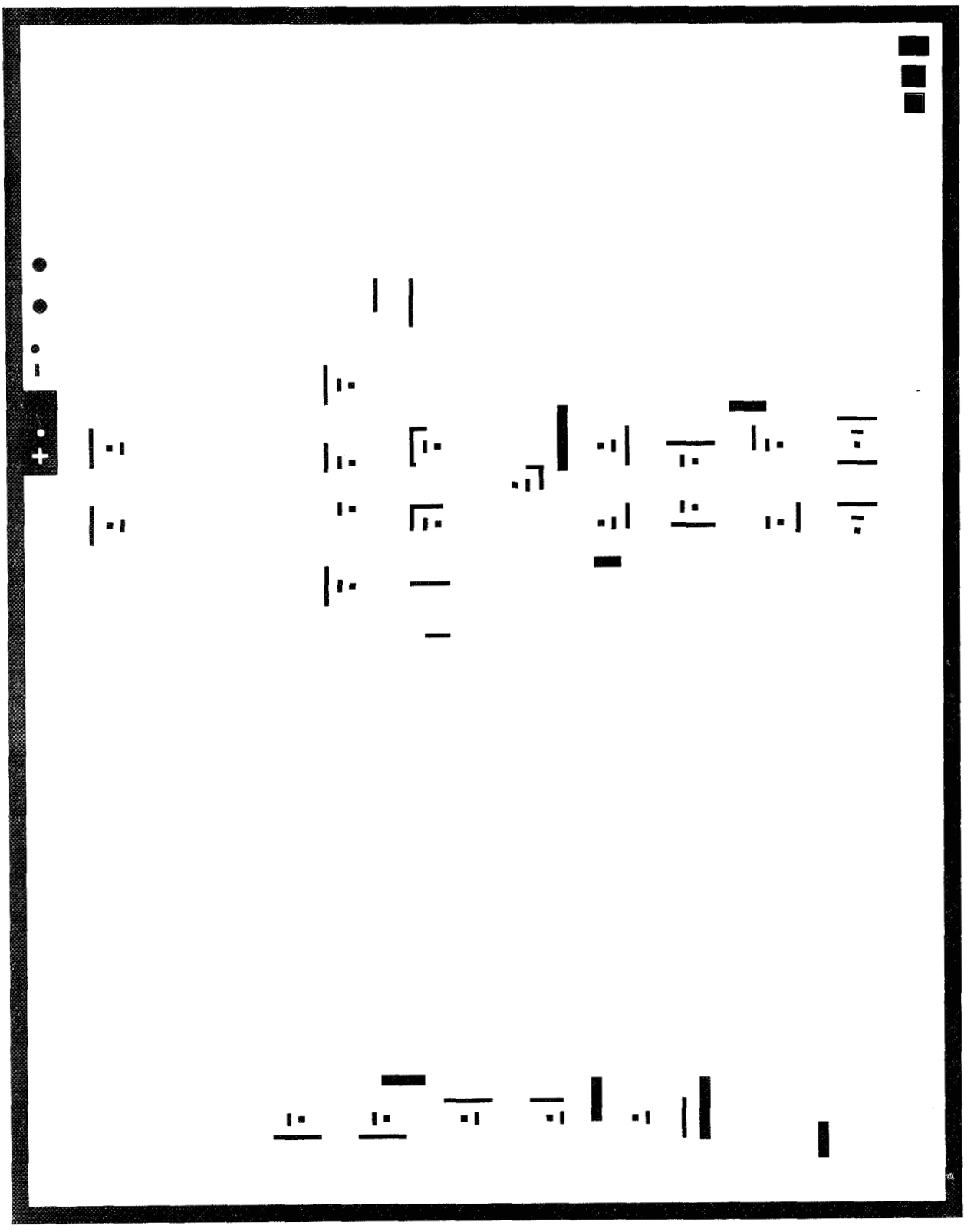


Figure 2-21. Contact

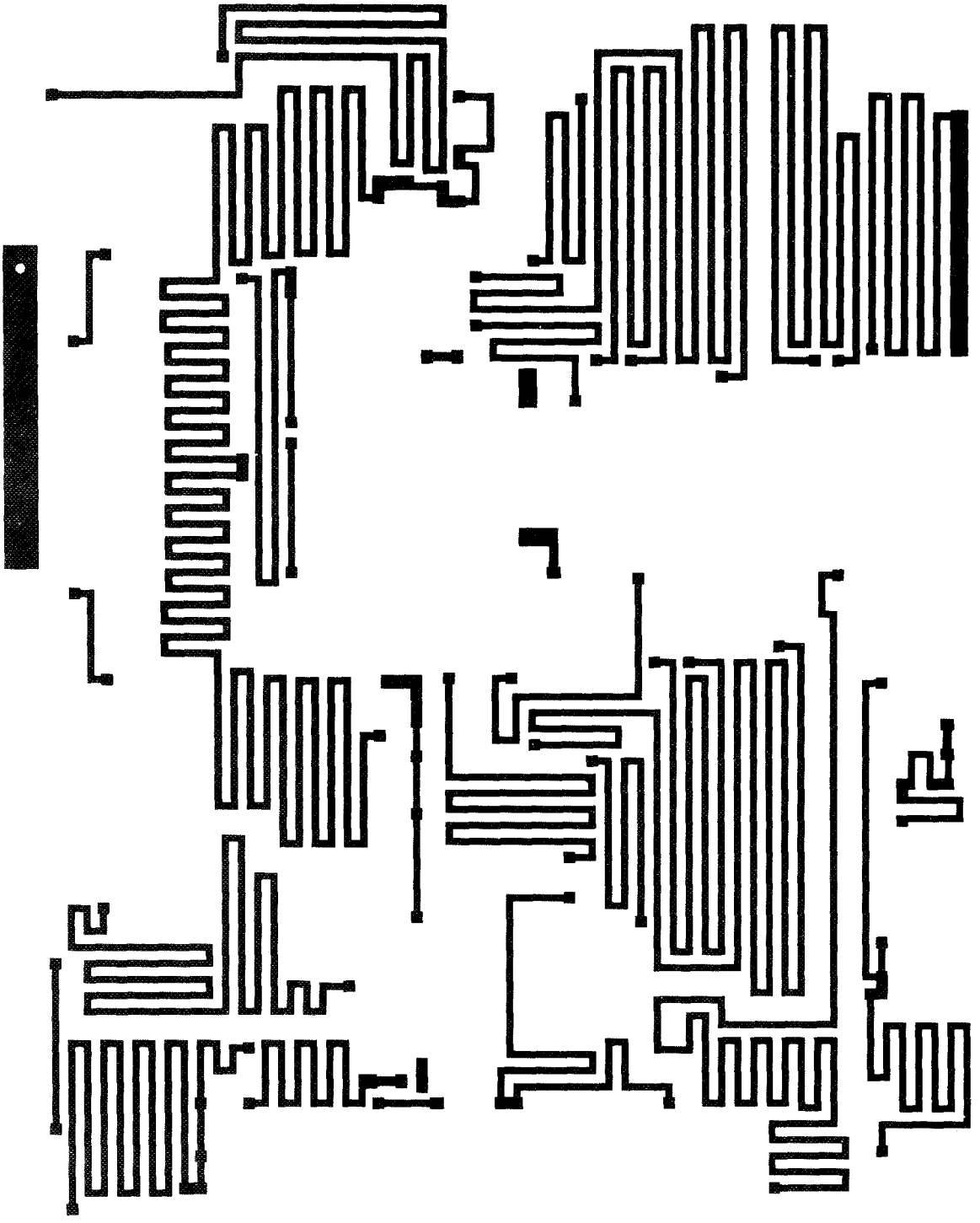


Figure 2-22. Cermet

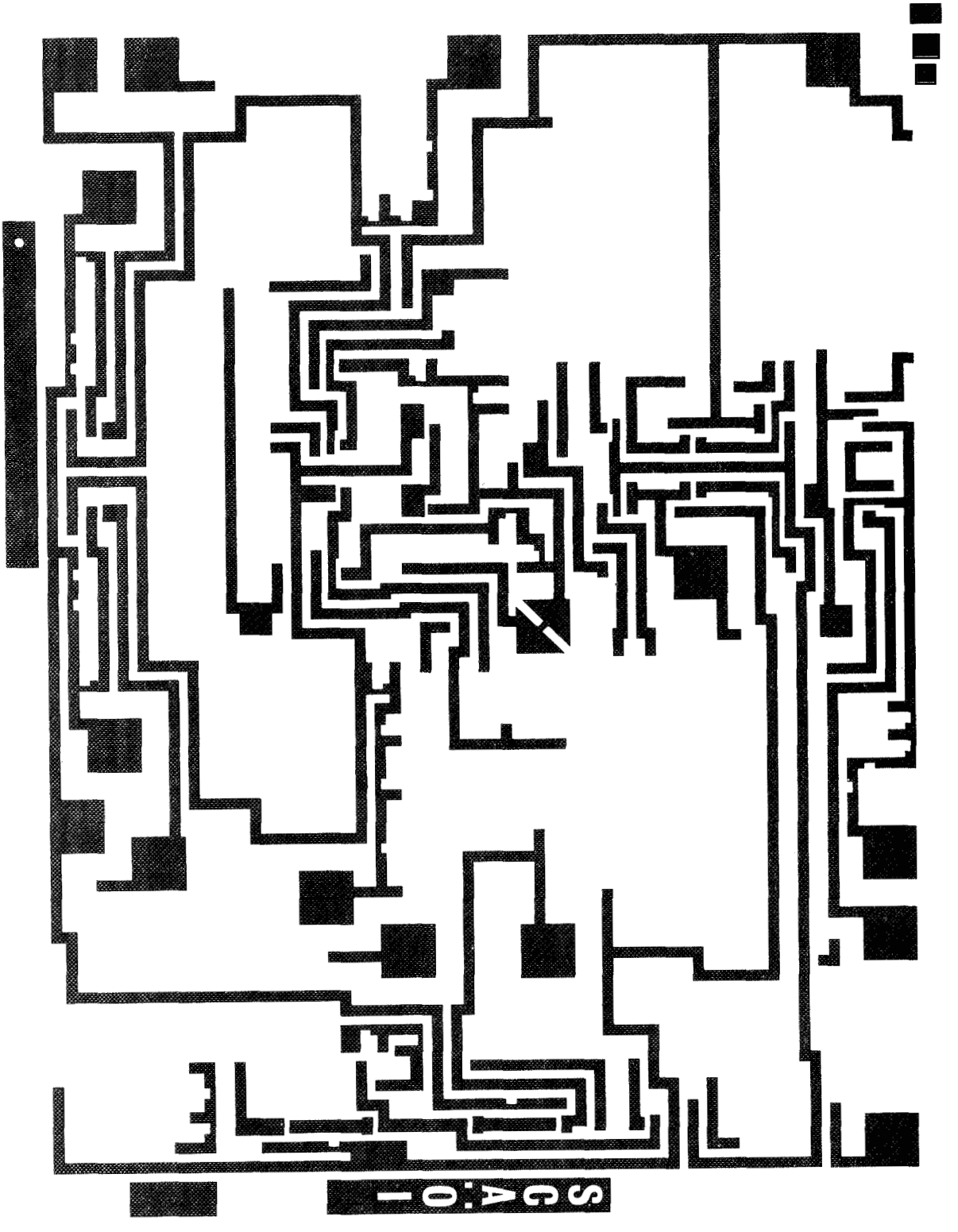


Figure 2-23. Metal Interconnect

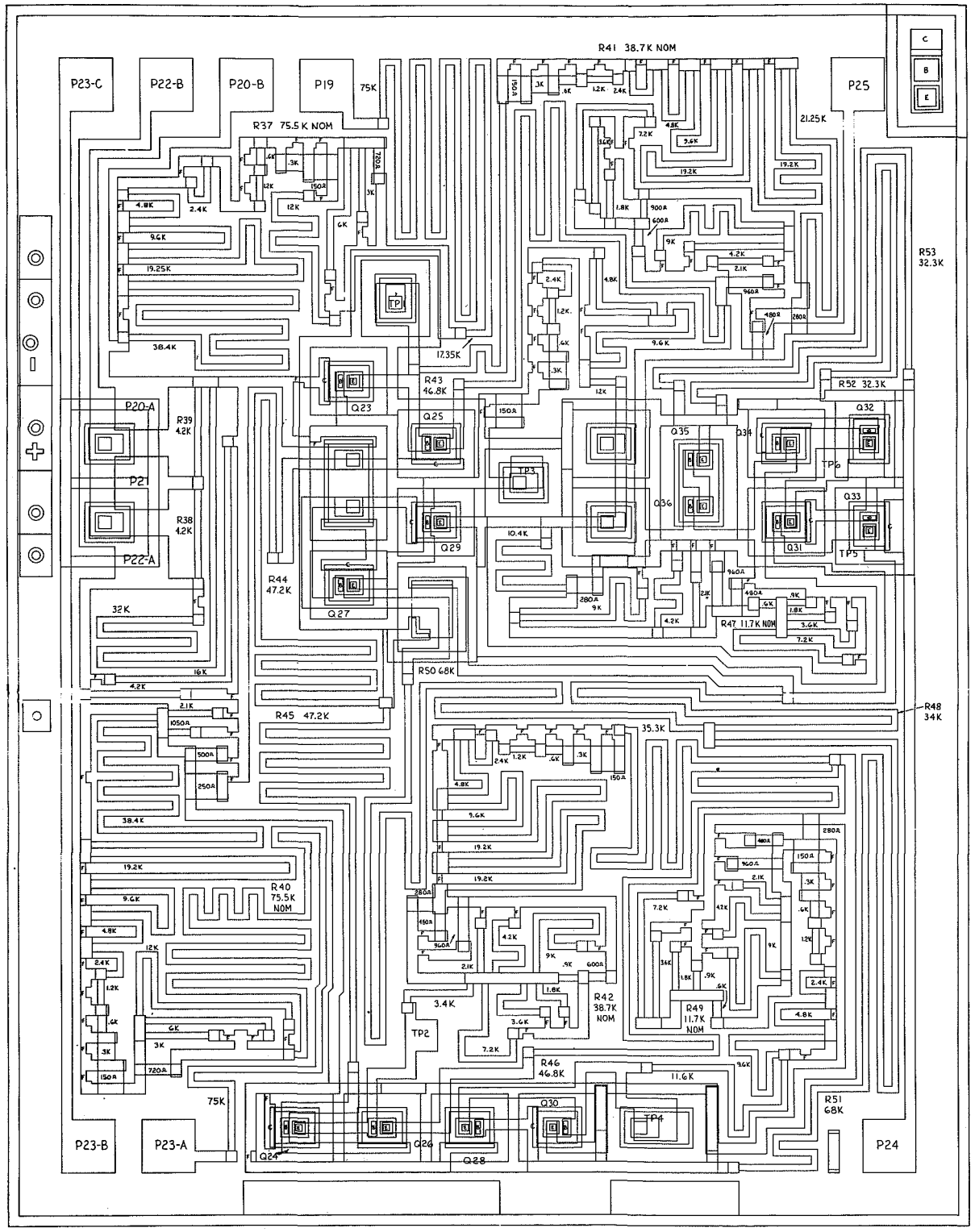


Figure 2-24. SCA42 Assembly Drawing

2.4 SUMMARY OF MEASURED PERFORMANCE DATA

With reference to Figure 2-10, as the input common-mode voltage changes, the currents in the feedback resistor network (R_{37}, R_{38}, R_{39}, and R_{40}) and resistor R_7 change. This, in turn, produces variations in the collector operating currents of the input stage, Q_1 and Q_2. The purpose of the common-mode feedback loop is to stabilize the operating currents of Q_1 and Q_2 in the environment of changing common-mode input voltages. Figure 2-25 shows data taken from the amplifier breadboard. This indicates a common-mode loop gain of about 900 and a common-mode input voltage operating range between -5 volts and +8 volts. Figure 2-26 shows the measured common-mode rejection as a function of frequency for closed loop gains of 1000 and 25. No attempt was made to optimize this characteristic by adjusting the feedback resistor. Note that the breadboard performance is considerably better than the 80 dB, 1 kHz specification.

The differential mode open loop gain is higher in this design than it was in the NAS 9-3410 design. Figure 2-27 shows the open loop gain as a function of temperature for closed loop gains of 1000 and 50. This indicates a closed loop gain variation of $\pm$0.15% for CLG = 1000, and $\pm$0.02% for CLG = 50. This performance is well within specification.

The linearity was measured and shown in Figure 2-28. In summary, over the operating output voltage range of 0 to +5 volts, the nonlinearity is less than 1 mV, again well within specification. The output voltage swing capability extends from -6 volts to +9 volts for a 25 k ohm load. The output circuit will drive 10,000 pF of capacitance. The output impedance is less than 0.1 ohm.

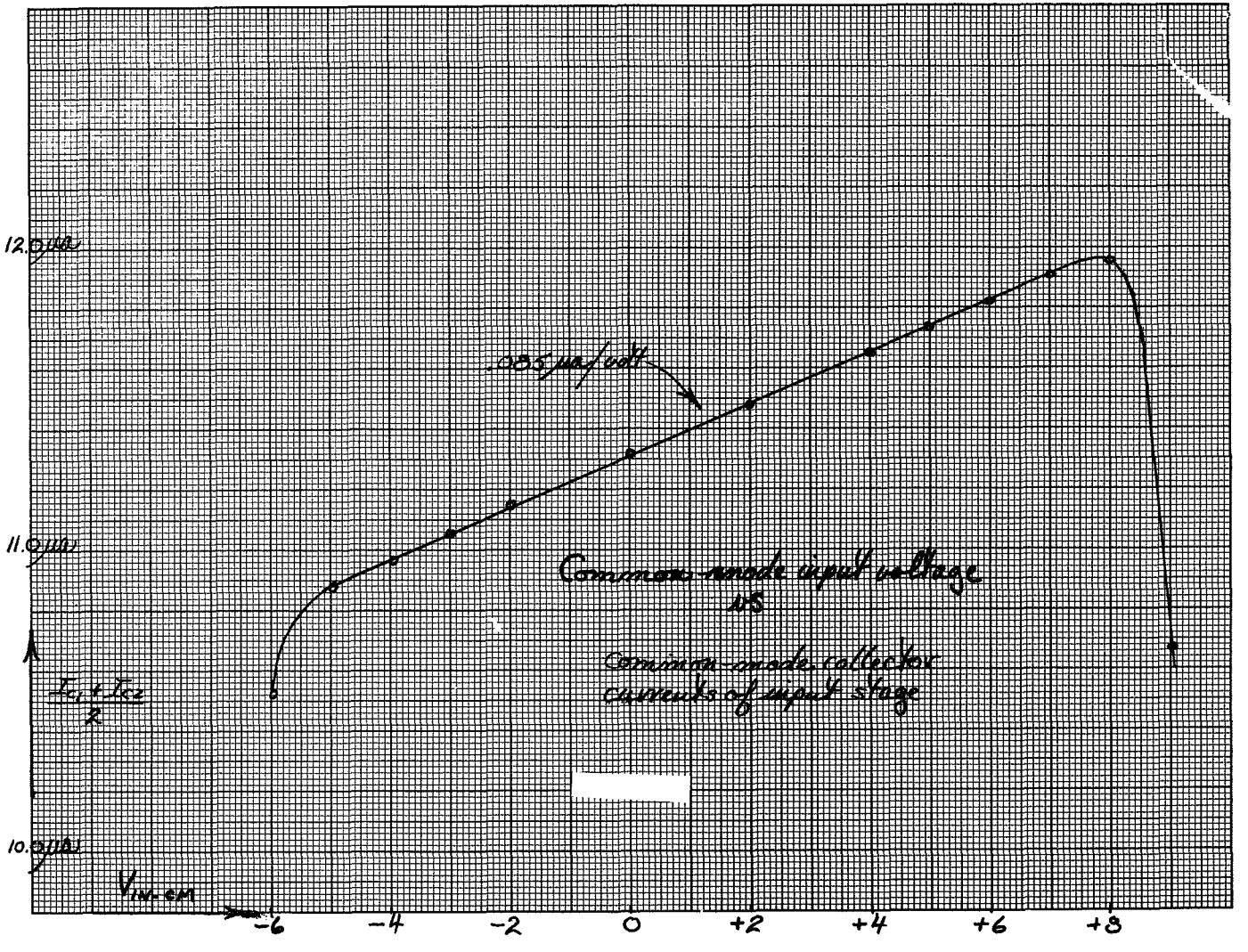
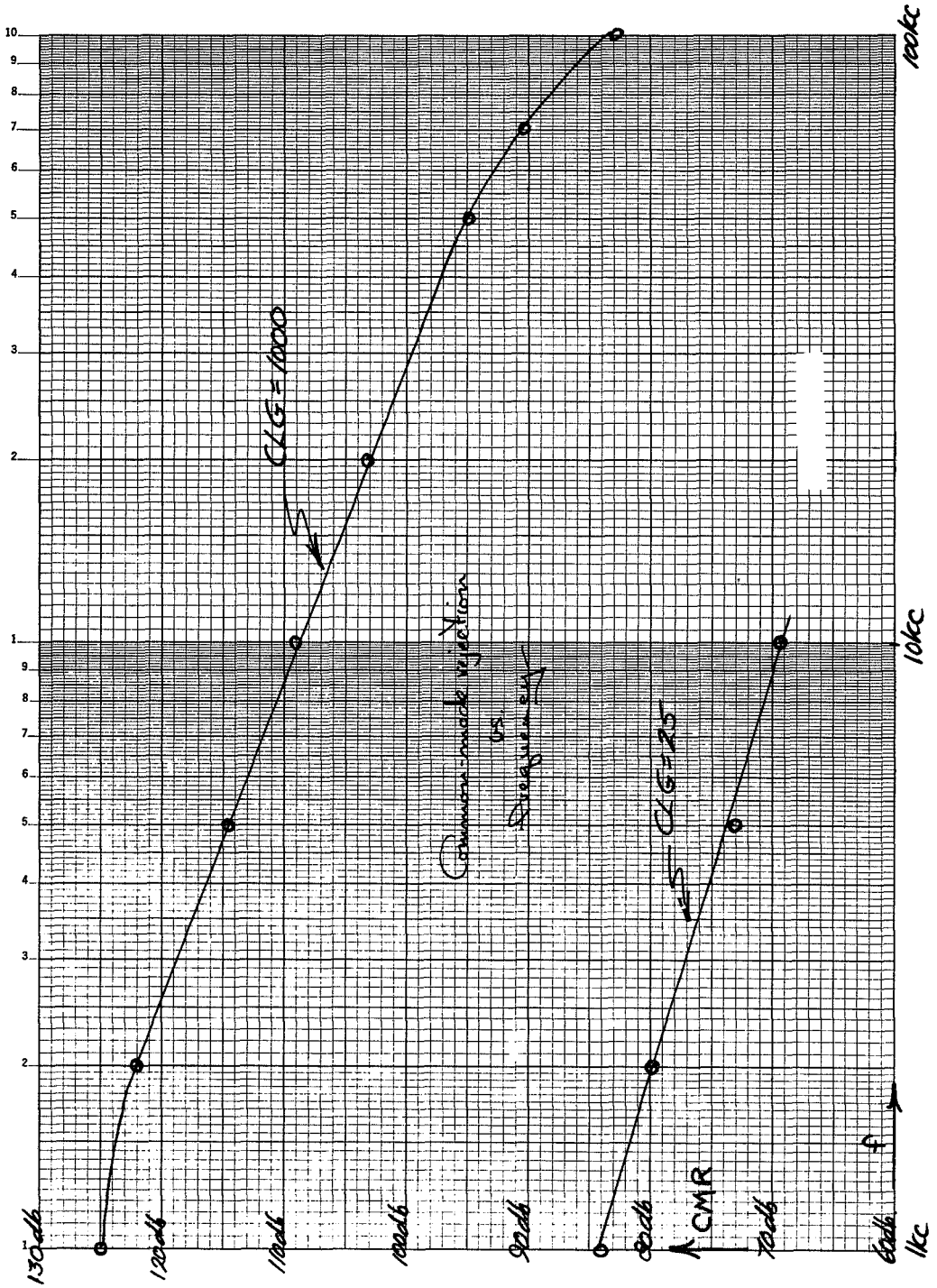
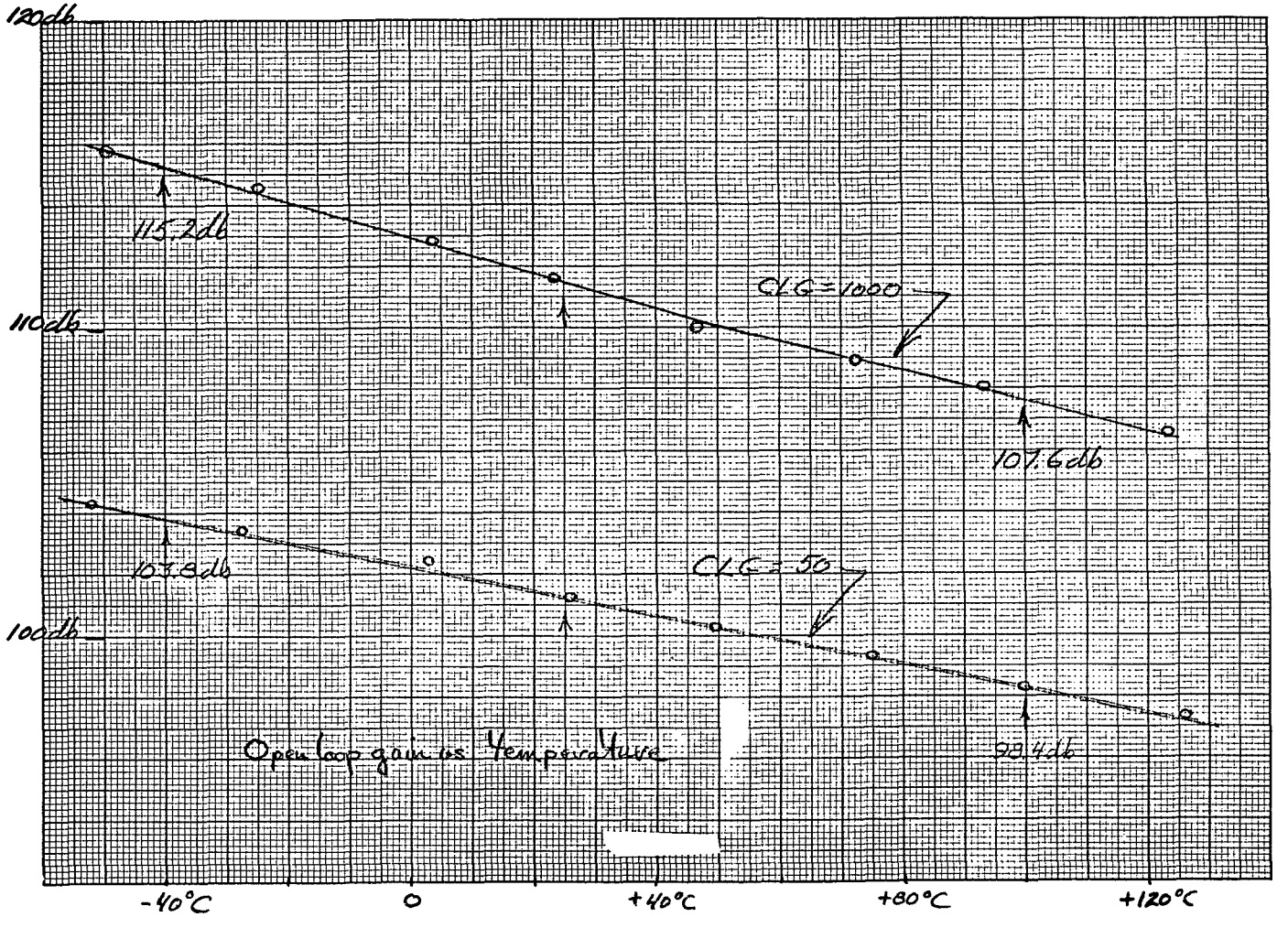


Figure 2-25. Common-Mode Performance


CLG=1000
CLG=25
CMR
Common-mode rejection
vs
Frequency
f
100kc
10kc
1kc
130db
120db
110db
100db
90db
80db
70db
60db


120db
110db
100db
115.2db
107.6db
107.8db
98.4db
CLG=1000
CLG=50
-40°C
0
+40°C
+80°C
+120°C
Open loop gain vs. Temperature

Linearity Measurements

CLG = 1000

R_L = 24K ohms to ground

$K \times V_{IN}$	$V_o - K \times V_{IN}$
0.	-1.051
1.0	-1.051
2.0	-1.051
3.0	-1.051
4.0	-1.051
5.0	-1.051
6.0	-1.051
7.0	-1.051
8.0	-1.052
9.0	-1.053
10.0	-1.061

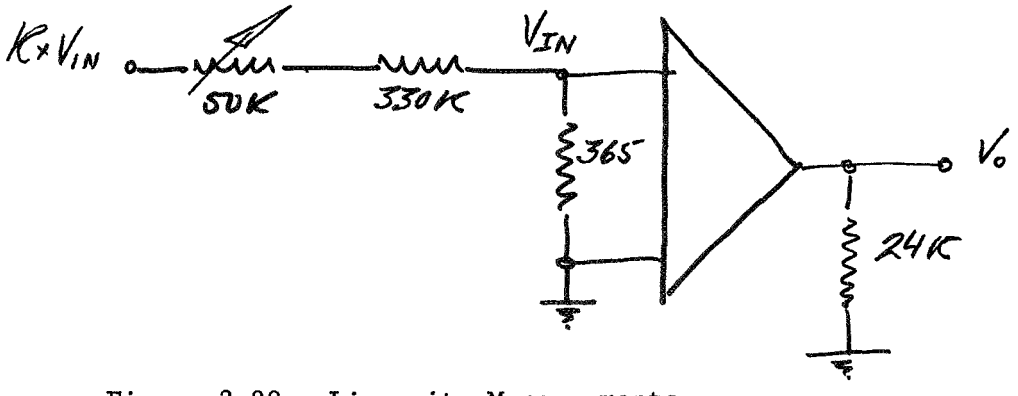


Figure 2-28. Linearity Measurements

The power gating characteristics of the breadboard amplifier were measured. A sketch of the test configuration and the wave shapes are shown in Figure 2-29. The GMR is turned on first, from t_3 to t_1, and then the GTR energizes the transducer from t_4 to t_1. The amplifier output transient at t_4 represents the turn-on time in interest, while the transient at t_1 represents the turn-off time. The output of the amplifier was monitored to determine the length of time needed for the amplifier to settle within 5 mV of its final value. Both the ON and OFF times were measured as 150μsec. These times were significantly reduced by removing all four 150 pF capacitors from the amplifier. Then, the $t_{ON} \simeq 15\mu sec$ and $t_{OFF} \simeq 60\mu sec$, assuming a 5 mV accuracy. The essential reason for the 150 pF capacitors is to minimize noise. If a 10 kHz filter is placed in the output circuit of the system, rather than in the low-level amplifier, these 150 pF capacitors could be removed.

Measured data taken on the integrated circuit amplifiers shipped on this contract is shown in Figures 2-30 through 2-49.

2.5 PACKAGING CONFIGURATIONS

Figure 2-50 illustrates the packaging option of mounting all the die in a 3/8" by 3/8" flat package. The capacitor die, in this case, has not been fabricated.

Figures 2-51, 2-52, and 2-53 show the option of mounting the SCA41, SCA42, and CA02 die in separate 1/4" by 3/8" flat packages. This is the form in which the amplifier was delivered on this contract.

Note: Appendix D shows the printed circuit board on which the amplifier modules were mounted.

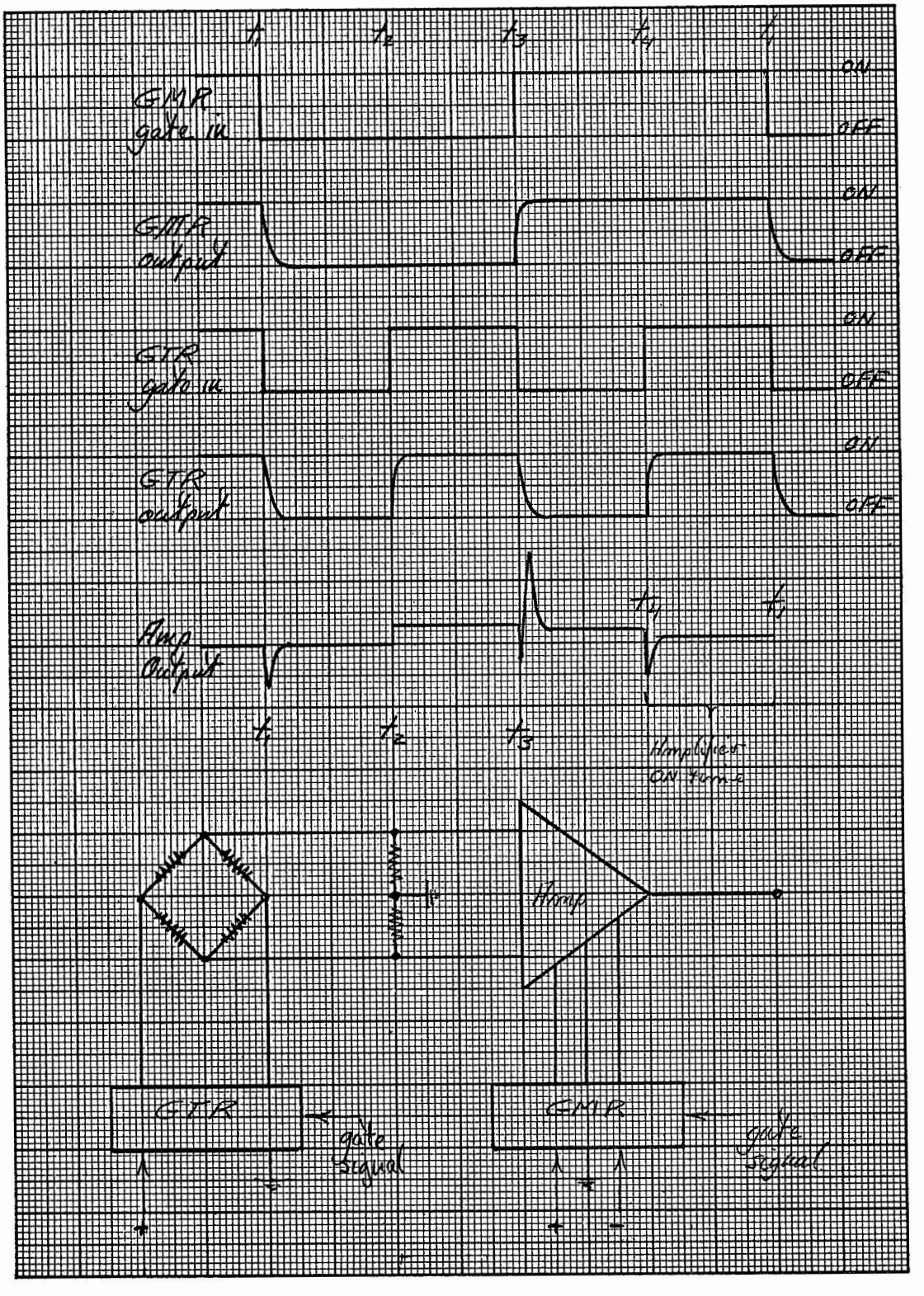


Figure 2-29. Test Configuration and Wave Shapes

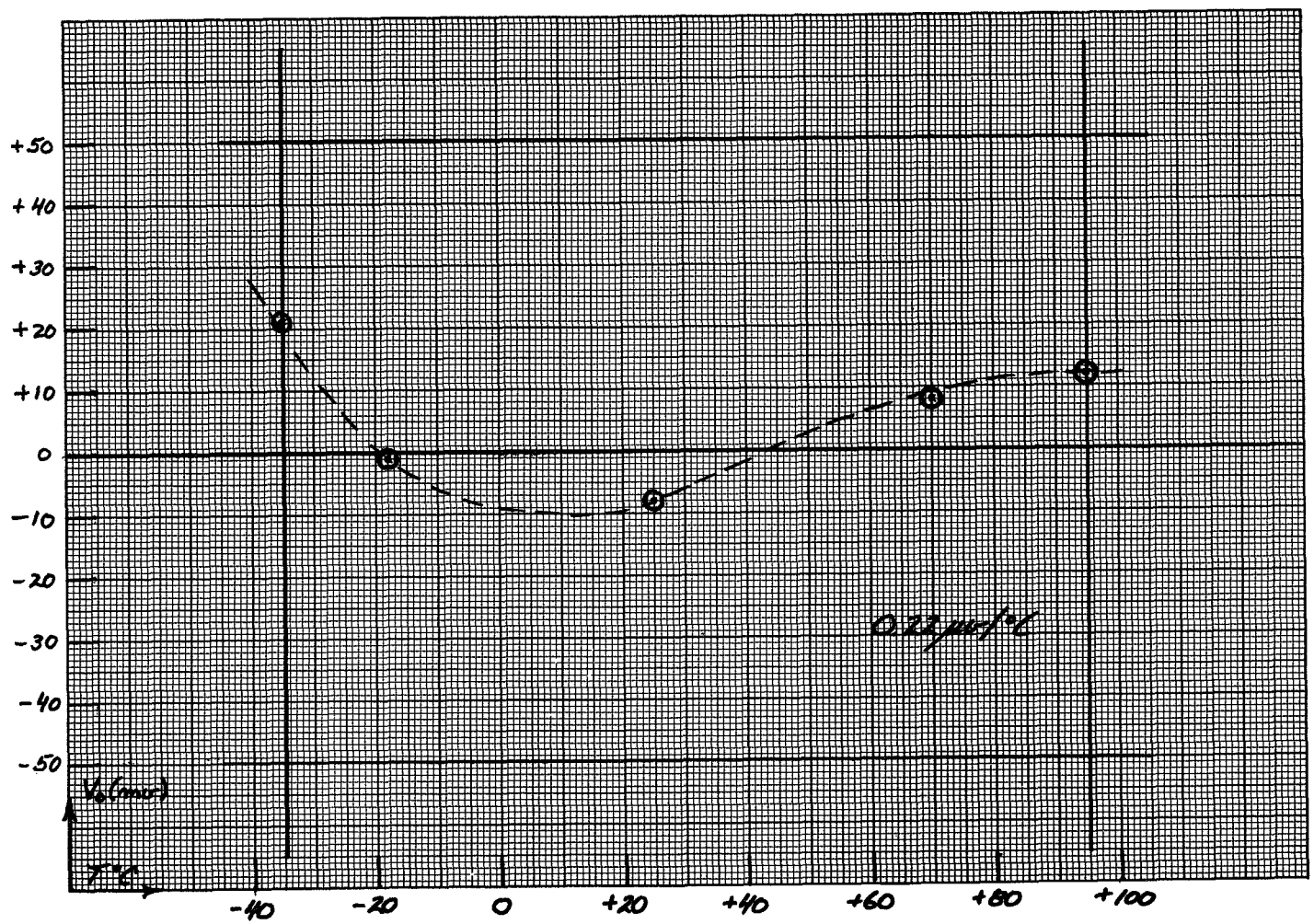


Figure 2-30. Amplifier 301 Output Offset

Amplifier No. 301 Nominal Gain 1000

Linearized drift referred to the input 0.22 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	+21	-8	+12	mv.
DC Gain	1004.2	1000.6	999.2	
Noise (referred to input)	9	20	10	μv. peak

+25°C Measurements

Linearity: Nominal Output	-1	0	+1	+2	+3	+4	+5	+6	(volts)
Deviation from Linearity	+1	0	+1	+1	+1	+1	0	0	(mv)

Frequency Response (3 db pt.) 5.3 kHz

Rolloff Rate 6 db per octave

Common mode rejection dc 98 db

1 kHz 98 db

Power supply rejection (+15) 11 μv/v referred to input

(-15) 10 μv/v referred to input

Figure 2-31. Amplifier 301 Measured Data

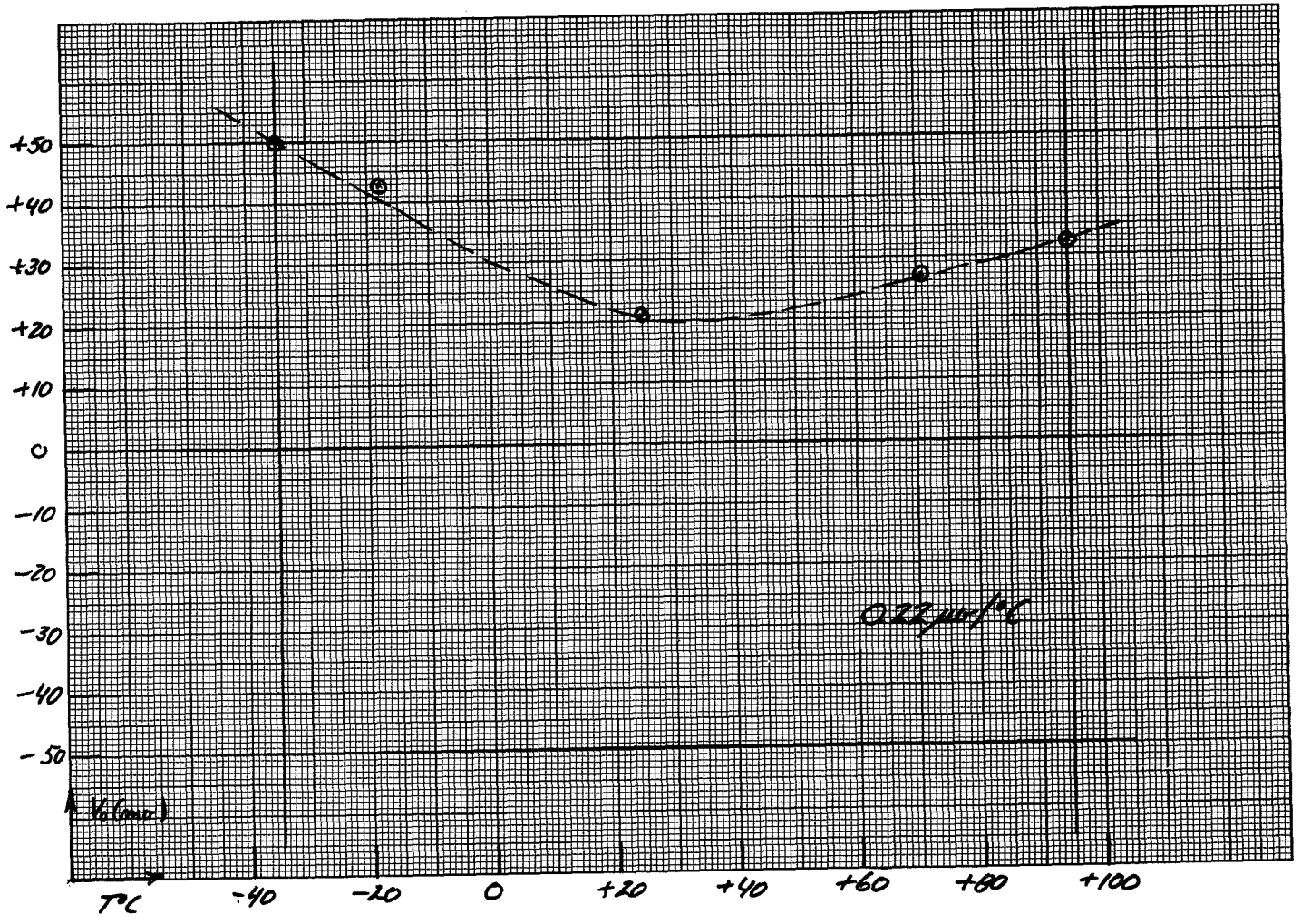


Figure 2-32. Amplifier 304 Output Offset

Amplifier No. 304 Nominal Gain 1000

Linearized drift referred to the input 0.22 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	+50	+21	+32	mv
DC Gain	990.0	987.9	987.4	
Noise (referred to input)	10	10	10	μv peak

+25°C Measurements

Linearity: Nominal Output	-1	0	+1	+2	+3	+4	+5	+6	(volts)
Deviation from Linearity	+1	0	0	+1	0	0	0	-1	(mv)

Frequency Response (3 db pt.) 4.5 kHz

Rolloff Rate 6 db per octave

Common mode rejection dc 118 db

1 kHz 102 db

Power supply rejection (+15) 18 μv/v referred to input

(-15) 17 μv/v referred to input

Figure 2-33. Amplifier 304 Measured Data

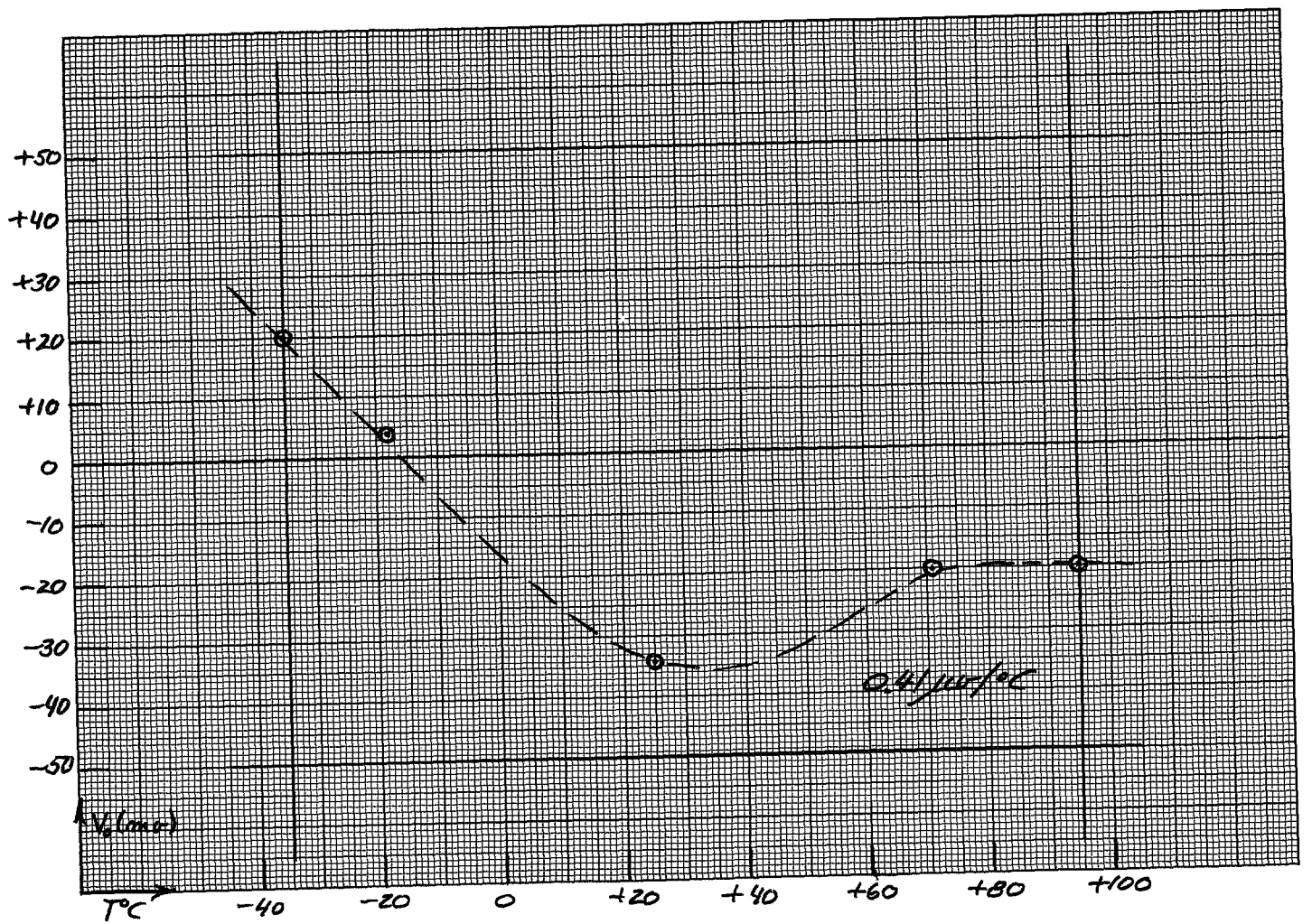


Figure 2-34. Amplifier 315 Output Offset

Amplifier No. 315 Nominal Gain 1000

Linearized drift referred to the input 0.41 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	+20	-34	-20	mv
DC Gain	1003.0	1000.6	998.2	
Noise (referred to input)	10	10	10	μv-peak

+25°C Measurements

Linearity:

Nominal Output	-1	0	+1	+2	+3	+4	+5	+6	(volts)
Deviation from Linearity	0	0	0	+1	+1	+1	+1	+1	(mv)

Frequency Response (3 db pt.) 6 kHz

Rolloff Rate 6 db per octave

Common mode rejection dc 114 db

1 kHz 118 db

Power supply rejection (+15) 25 μv/v referred to input

(-15) 32 μv/v referred to input

Figure 2-35. Amplifier 315 Measured Data

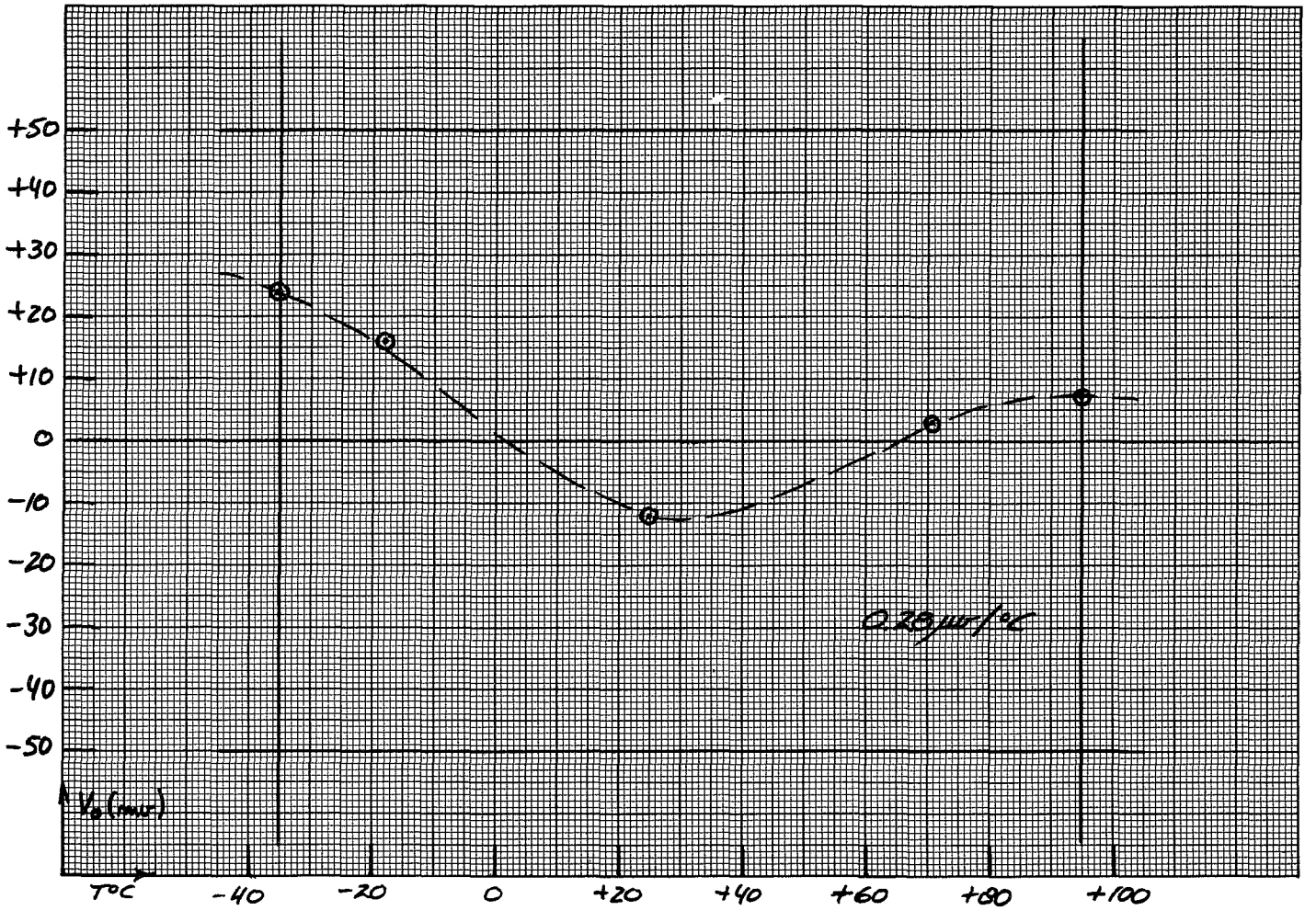


Figure 2-36. Amplifier 308 Output Offset

Amplifier No. 308 Nominal Gain 1000

Linearized drift referred to the input 0.28 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	+24	-12	+7	mv
DC Gain	998.2	998.4	999.4	
Noise (referred to input)	10	10	10	μv peak

+25°C Measurements

Linearity: Nominal Output	-1	0	+1	+2	+3	+4	+5	+6	(volts)
Deviation from Linearity	-6	0	+1	+3	+6	+8	+1	-7	(mv)

Frequency Response (3 db pt.) 5.7 kHz

Rolloff Rate 6 db per octave

Common mode rejection dc 108 db

1 kHz 110 db

Power supply rejection (+15) 40 μv/v referred to input

(-15) 29 μv/v referred to input

Figure 2-37. Amplifier 308 Measured Data

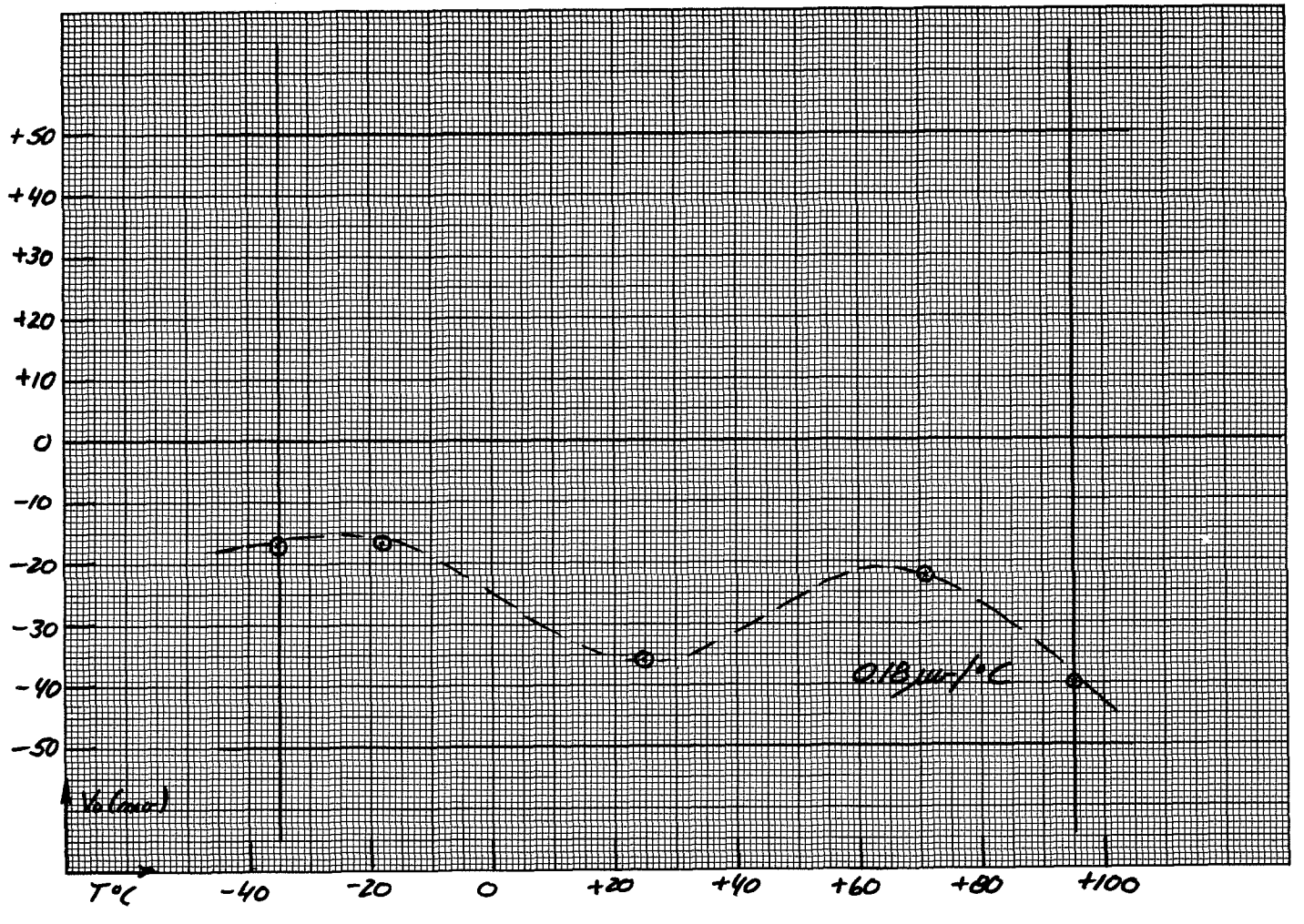


Figure 2-38. Amplifier 319 Output Offset

Amplifier No. 319 Nominal Gain 1000

Linearized drift referred to the input 0.18 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	-17	-36	-40	mv
DC Gain	1002.2	1001.4	999.0	
Noise (referred to input)	10	10	10	μv peak

+25°C Measurements

Linearity: Nominal Output -1 0 +1 +2 +3 +4 +5 +6 (volts)

Deviation from Linearity -1 0 0 0 0 0 0 -1 (mv)

Frequency Response (3 db pt.) 8 kHz

Rolloff Rate 6 db per octave

Common mode rejection dc 112 db

1 kHz 114 db

Power supply rejection (+15) 36 μv/v referred to input

(-15) 24 μv/v referred to input

Figure 2-39. Amplifier 319 Measured Data

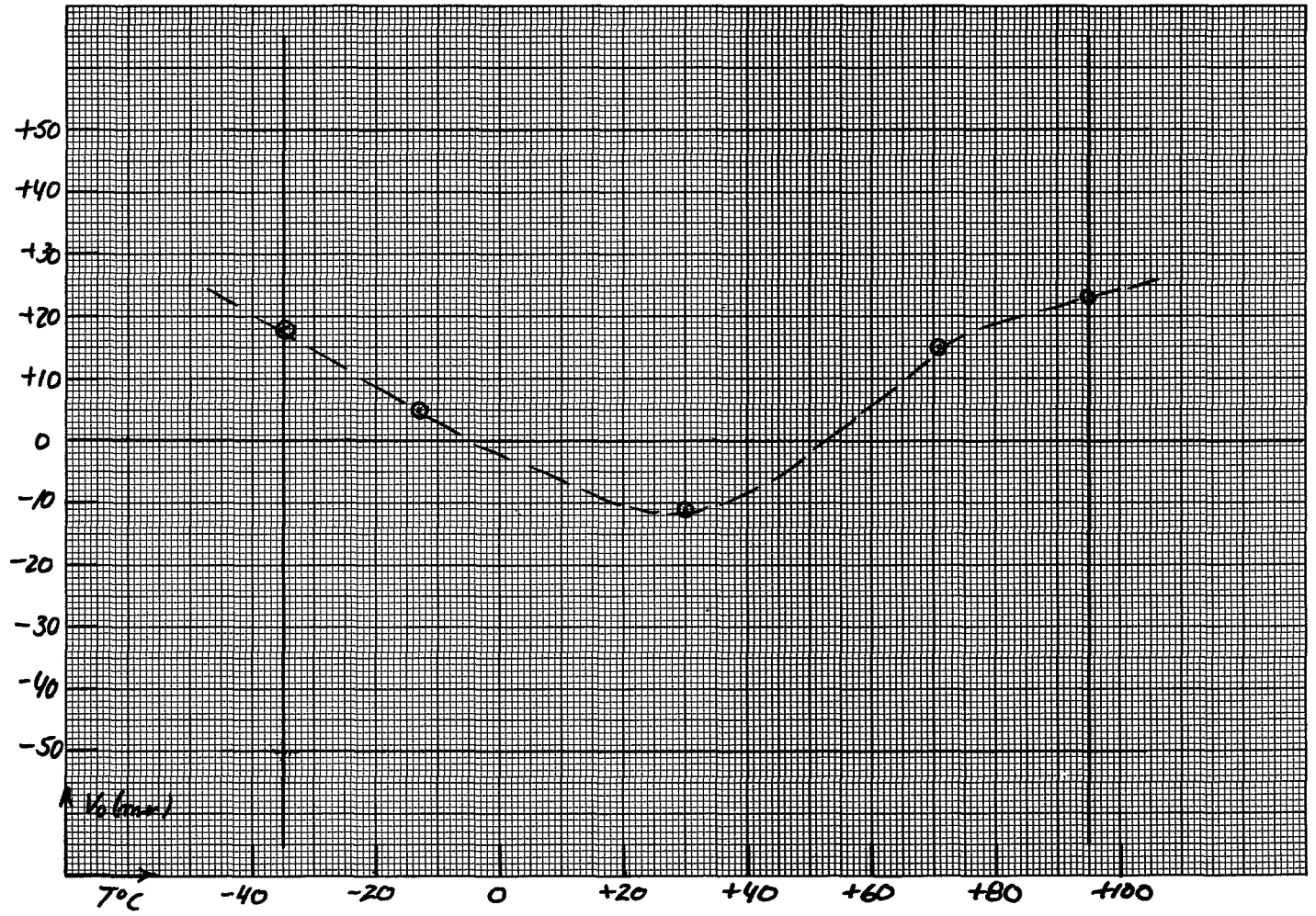


Figure 2-40. Amplifier 401 Output Offset

Amplifier No. 401 Nominal Gain 50

Linearized drift referred to the input 5.2 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	+18	-11	+23	mv
DC Gain	50.18	50.20	50.26	
Noise (referred to input)	10	9	10	μv peak

+25°C Measurements

Linearity: Nominal Output	-1	0	+1	+2	+3	+4	+5	+6	(volts)
Deviation from Linearity	0	0	0	0	+1	+1	+2	+3	(mv)

Frequency Response (3 db pt.) 8 kHz

Rolloff Rate 6 db per octave

Common mode rejection dc 102 db

1 kHz 100 db

Power supply rejection (+15) 60 μv/v referred to input

(-15) 40 μv/v referred to input

Figure 2-41. Amplifier 401 Measured Data

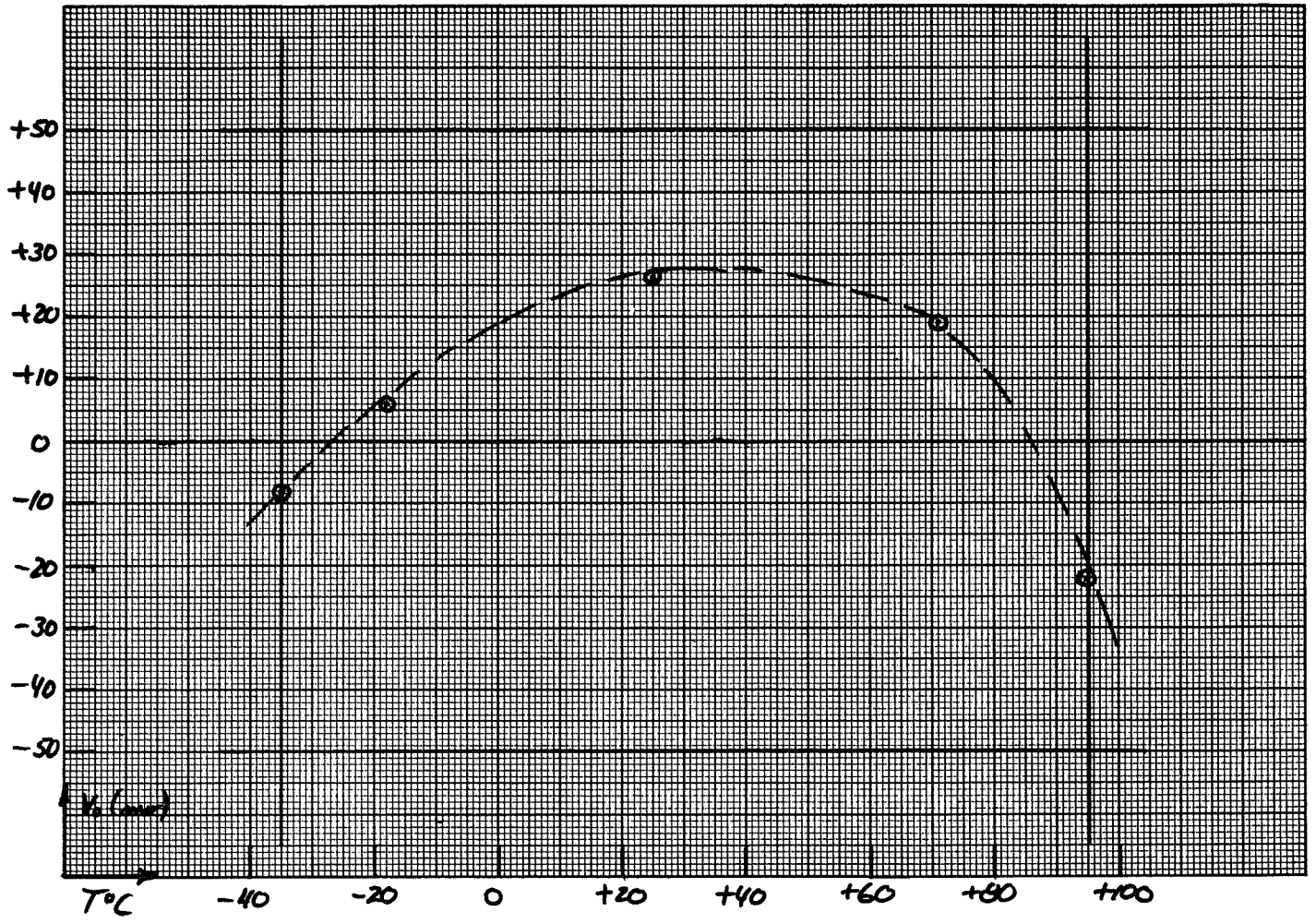


Figure 2-42. Amplifier 402 Output Offset

Amplifier No. 402 Nominal Gain 50

Linearized drift referred to the input 7.0 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	-8	+26	-22	mv
DC Gain	49.89	49.95	49.93	
Noise (referred to input)	10	3	10	μv peak

+25°C Measurements

Linearity: Nominal Output	-1	0	+1	+2	+3	+4	+5	+6	(volts)
Deviation from Linearity	-2	0	+1	+1	+2	+3	+3	+4	(mv)

Frequency Response (3 db pt.) 9 kHz

Rolloff Rate 6 db per octave

Common mode rejection dc 84 db

1 kHz 83 db

Power supply rejection (+15) 40 μv/v referred to input

(-15) 80 μv/v referred to input

Figure 2-43. Amplifier 402 Measured Data

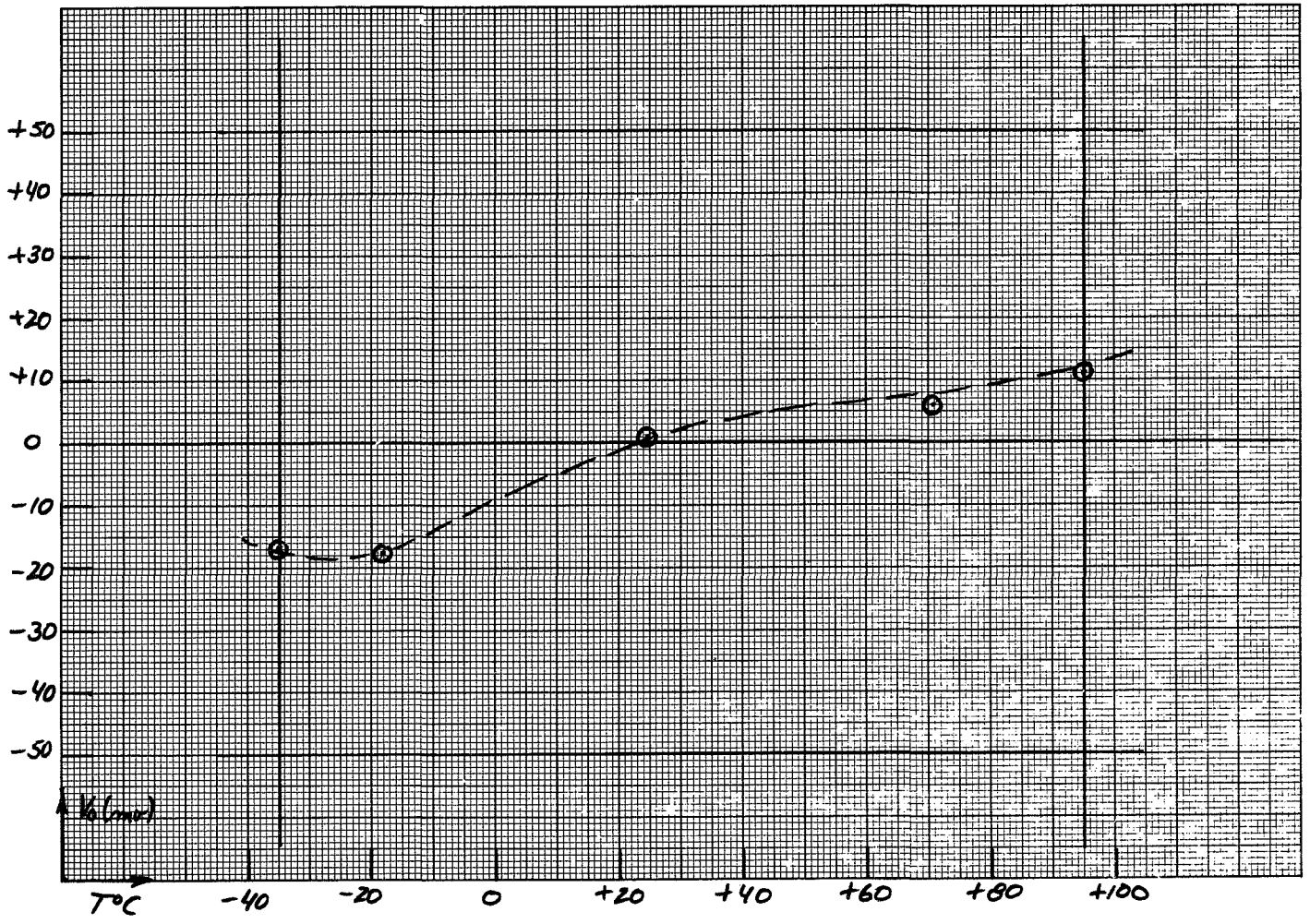


Figure 2-44. Amplifier 406 Output Offset

Amplifier No. 406 Nominal Gain 50

Linearized drift referred to the input 4.4 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	-17	+1	+11	mv
DC Gain	50.03	50.10	50.15	
Noise (referred to input)	10	5	10	μv peak

+25°C Measurements

Linearity: Nominal Output	-1	0	+1	+2	+3	+4	+5	+6	(volts)
Deviation from Linearity	0	0	0	0	-1	-1	0	0	(mv)

Frequency Response (3 db pt.) 9 kHz

Rolloff Rate 6 db per octave

Common mode rejection dc 78 db

1 kHz 76 db

Power supply rejection (+15) 160 μv/v referred to input

(-15) 140 μv/v referred to input

Figure 2-45. Amplifier 406 Measured Data

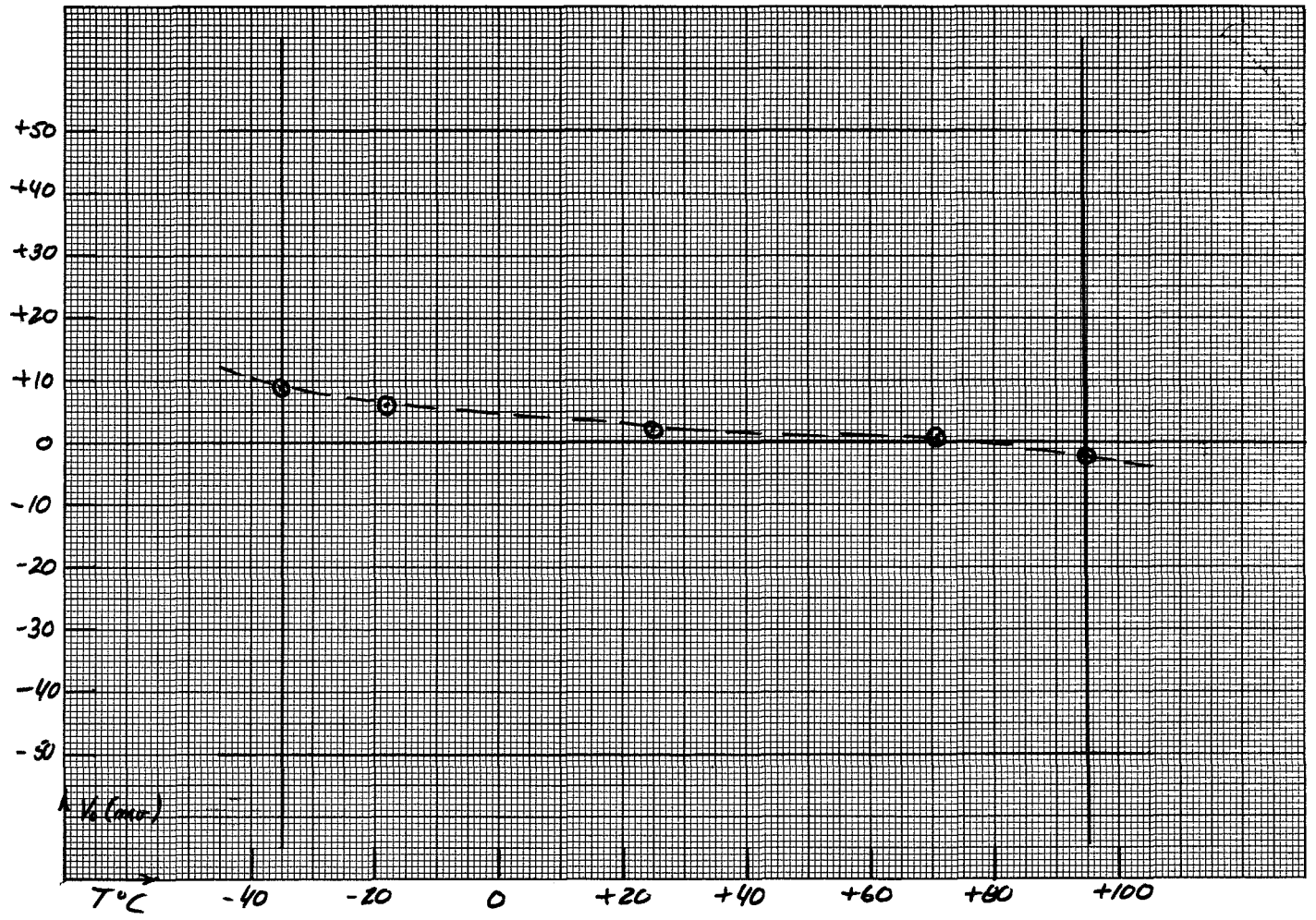


Figure 2-46. Amplifier 408 Output Offset

Amplifier No. 408 Nominal Gain 50

Linearized drift referred to the input 1.7 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	+9	+2	-2	mv
DC Gain	49.96	50.03	50.10	
Noise (referred to input)	10	5	10	μv peak

+25°C Measurements

Linearity: Nominal Output	-1	0	+1	+2	+3	+4	+5	+6	(volts)
Deviation from Linearity	0	0	0	0	0	0	0	0	(mv)

Frequency Response (3 db pt.) 9 kHz

Rolloff Rate _____ db per octave

Common mode rejection dc 102 db

1 kHz 89 db

Power supply rejection (+15) 60 μv/v referred to input

(-15) 60 μv/v referred to input

Figure 2-47. Amplifier 408 Measured Data

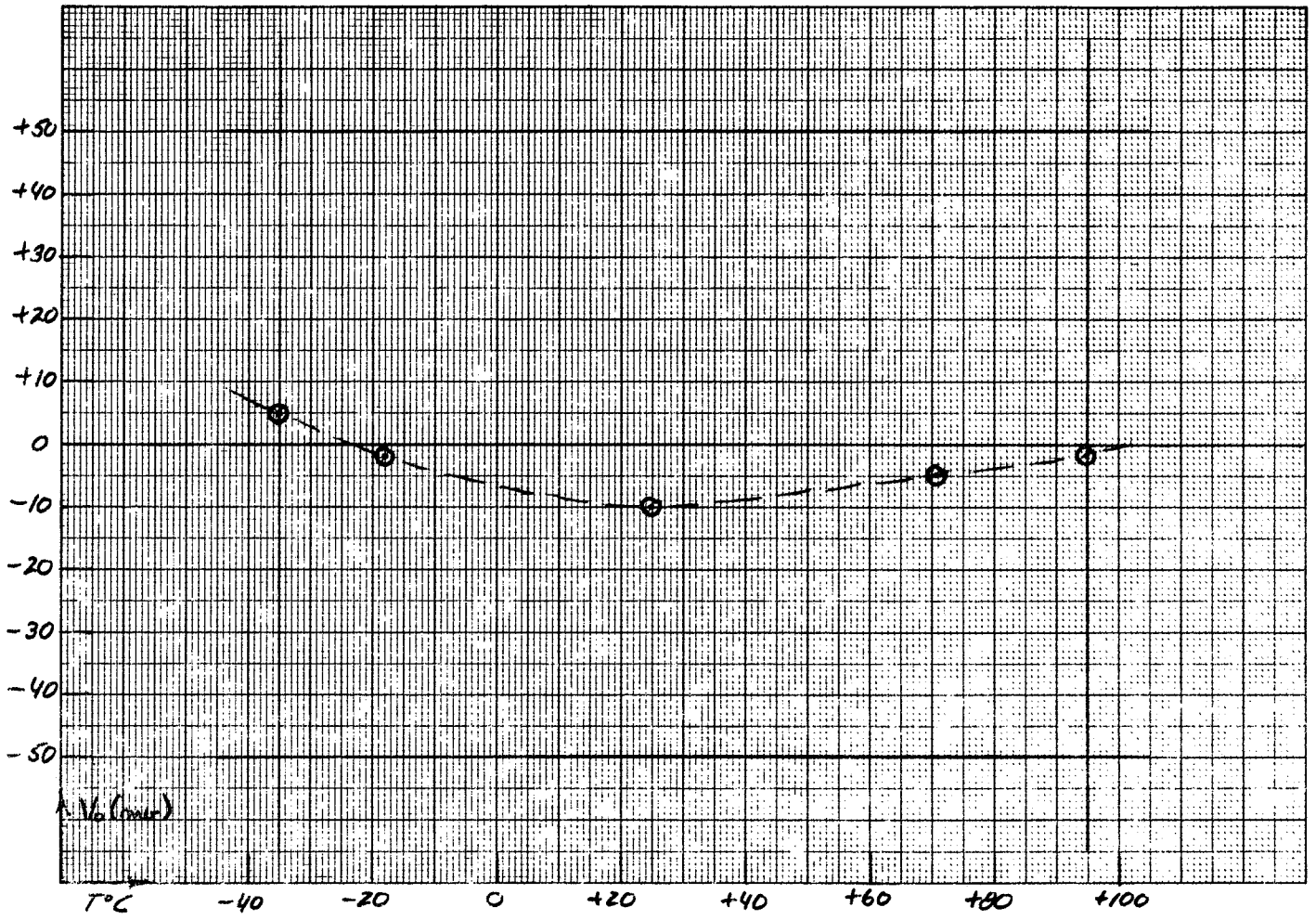


Figure 2-48. Amplifier 411 Output Offset

Amplifier No. 411 Nominal Gain 50

Linearized drift referred to the input 2.3 μv/°C.

	-35°C	+25°C	+95°C	
Output Offset	+5	-10	-2	mv
DC Gain	49.89	49.91	49.93	
Noise (referred to input)	5	10	10	μv peak

+25°C Measurements

Linearity: Nominal Output	-1	0	+1	+2	+3	+4	+5	+6	(volts)
Deviation from Linearity	0	0	0	+1	+1	+1	+1	+2	(mv)

Frequency Response (3 db pt.) 9 kHz

Rolloff Rate 6 db per octave

Common mode rejection dc 104 db

1 kHz 92 db

Power supply rejection (+15) 40 μv/v referred to input

(-15) 40 μv/v referred to input

Figure 2-49. Amplifier 411 Measured Data

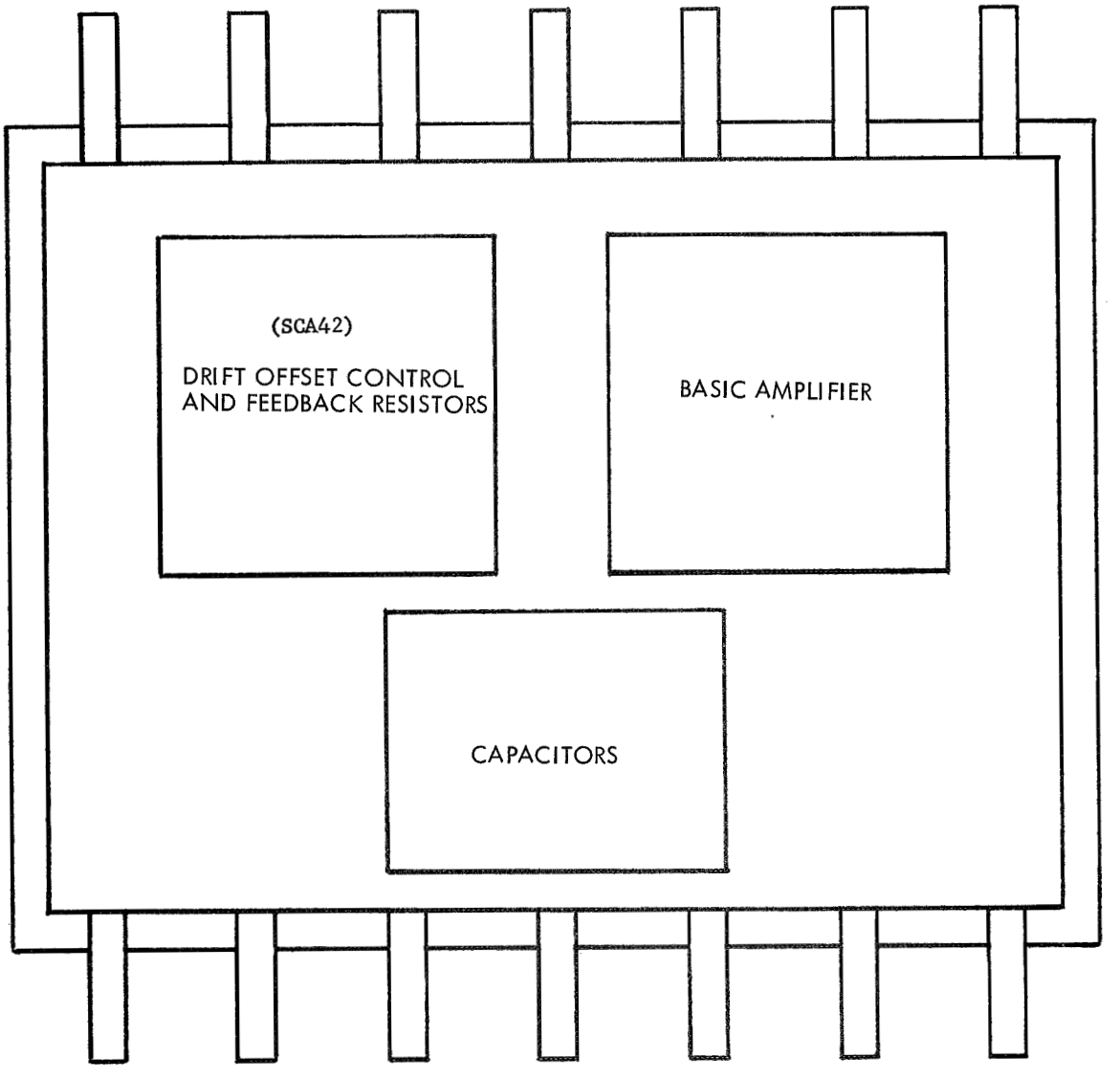


Figure 2-50. Sketch of Single Package Configuration

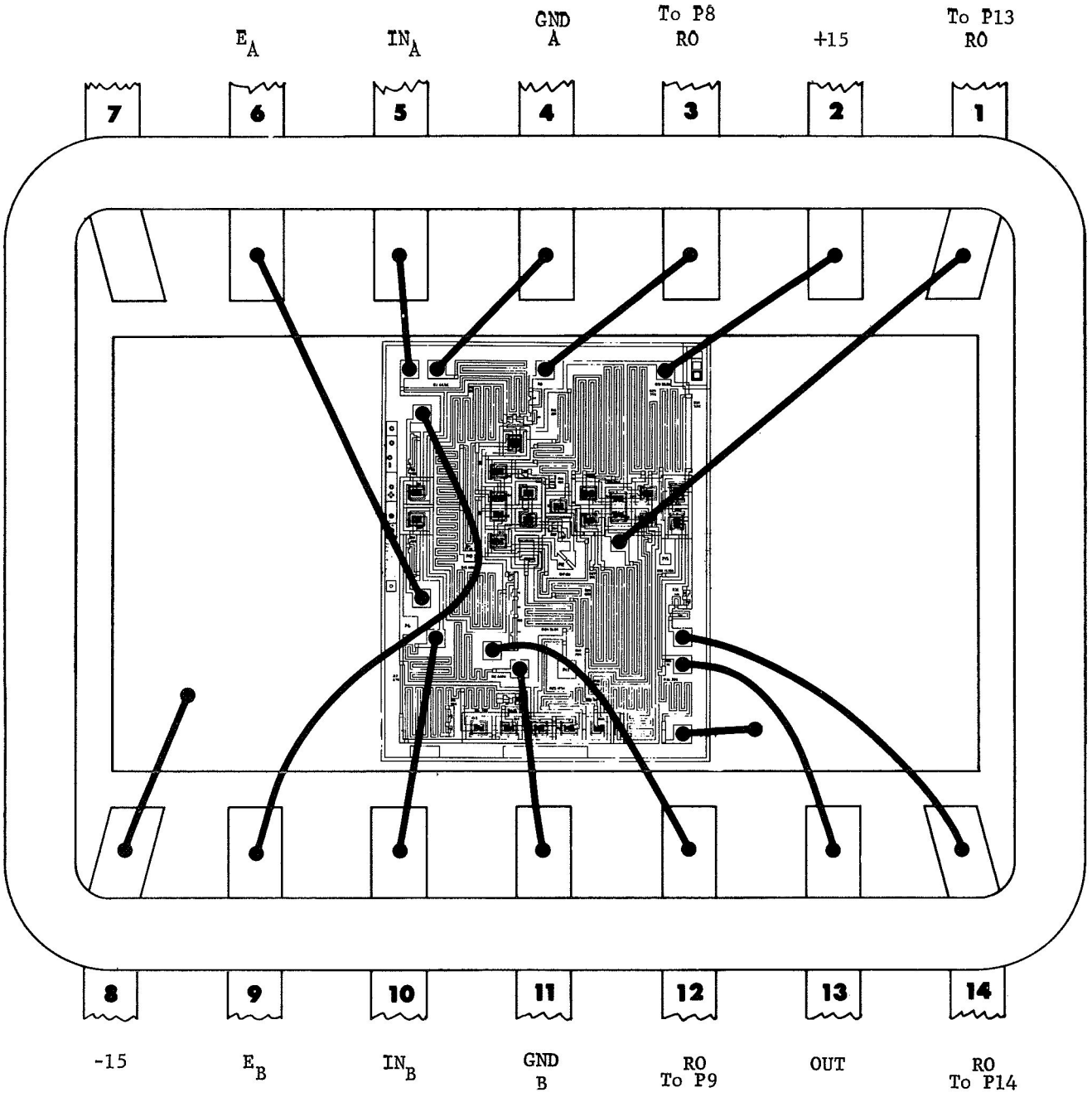


Figure 2-51. SCA41 Package

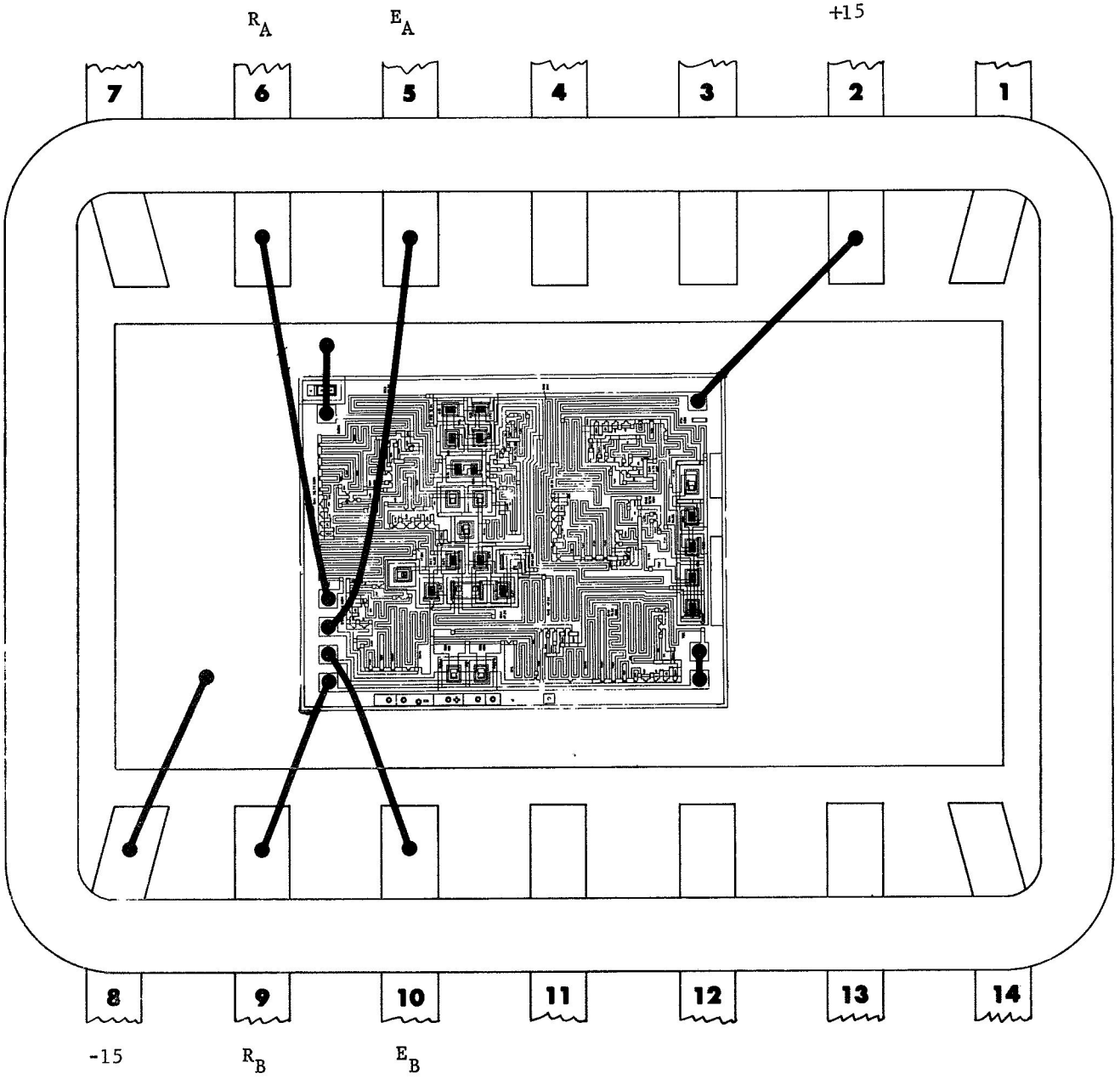


Figure 2-52. SCA42 Package

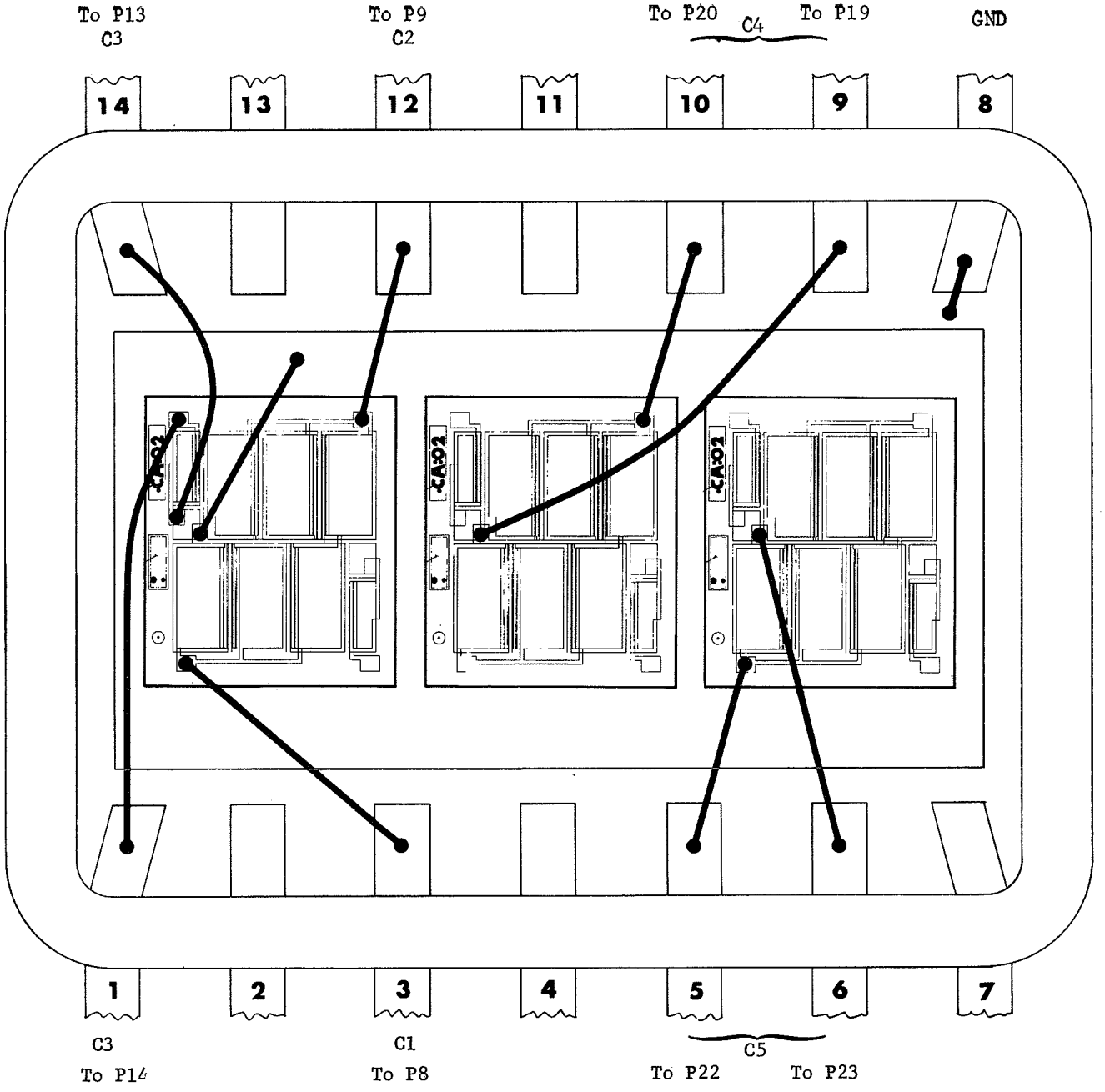


Figure 2-53. CA02 Package

3. POWER SOURCE

3.1 GENERAL

The power source converts the 28-volt unregulated battery voltage into three regulated voltages; V_1 to power the transducer and V_2 and V_3 to power the amplifiers. Figure 3-1 shows the block configuration.

A microminiature power converter provides electrical isolation (transformer coupling) and preregulation. This direct compensation pulsewidth modulation converter operates at 200 kHz switching rate. No overall feedback loop is used. The four converter outputs are further conditioned by the VR34 and VR35 series regulators to insure excellent line regulation and ripple rejection. If overall feedback is included in the converter (as proposed future models will), these series regulators will not be required, thereby increasing the efficiency of the power source. Table 3-I gives the input-output specifications of the power source.

a) Input - The power source shall be powered from an external battery. The characteristics of this battery are as follows:

- o The voltage is between 22 and 32 volts with 28 volts being nominal.
- o There is a possible maximum 4 volt peak-to-peak ripple (dc to 2 kHz square wave) impressed upon the battery voltage. The battery voltage, including the ripple, will be between 22 and 32 volts.
- o There is a possible transient on the power line that may reduce the battery voltage to as low as 0 volts or increase it to as high as 43 volts. This transient has a 20 millisecond basewidth duration and an 8 millisecond rise time.
- o The circuitry connected to the battery is required to survive this transient, but the specification performance is not required. Operation shall return to normal within 100 microseconds after the duration of the pulse.

b) Output - The output characteristics are shown in Table 3-I.

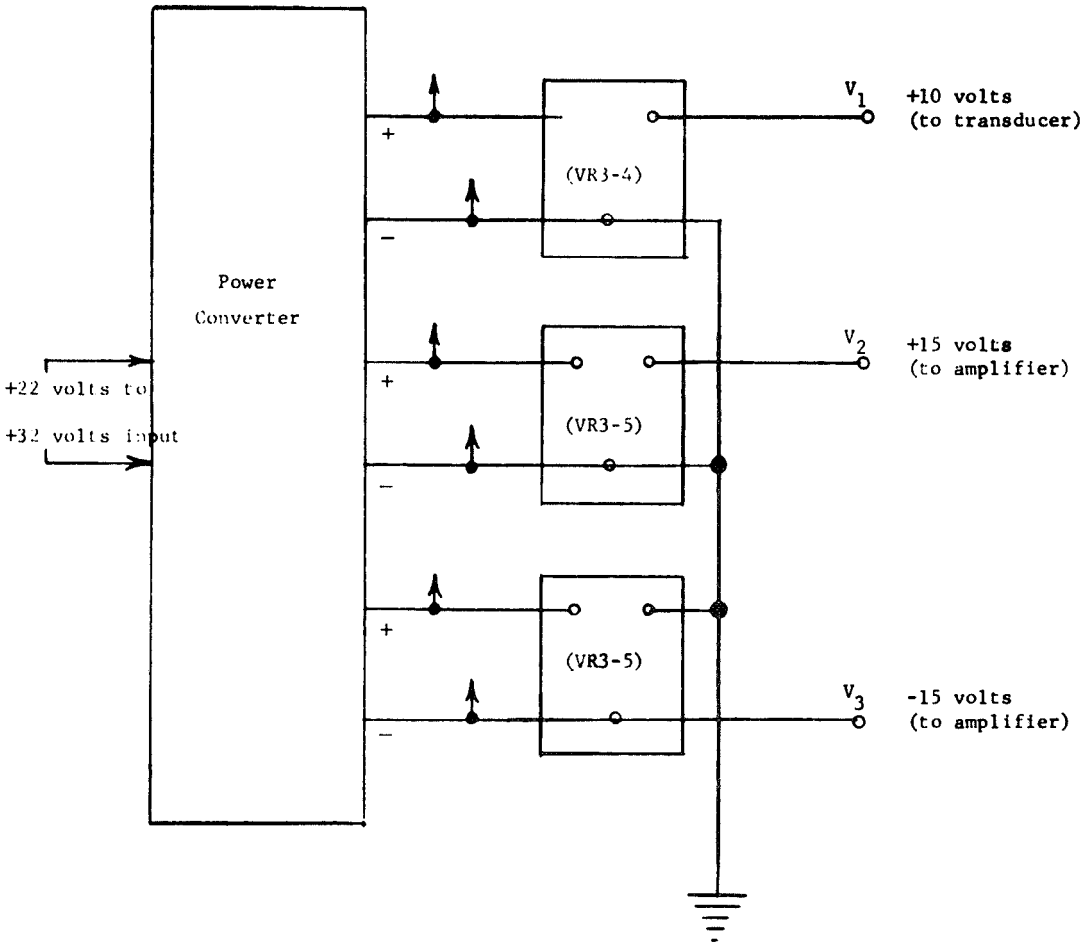


Figure 3-1. Signal Conditioner Power Source

TABLE 3-I. POWER SOURCE INPUT/OUTPUT SPECIFICATIONS

	Voltage			Current Drawn
	Minimum	Typical	Maximum	Typical
V_1	9.950	10.000	10.050	30 mA
V_2	14.9	15.0	15.1	6 mA
V_3	14.9	15.0	15.1	6 mA

The minimum-typical-maximum output voltage specifications include effects due to line, load, and temperature variations in addition to initial setting.

3.2 POWER CONVERTER

3.2.1 Description

Figures 3-2 and 3-3 show, respectively, a block diagram and a schematic diagram of the power converter. This unit is designed to supply a total of 3 watts. The circuit, consisting of an input filter, a reference supply, a timing oscillator, and a power output stage, comprises a self-regulating converter which combines the functions of inversion, line regulation, rectification, and filtering.

The theory of operation of this circuit can best be described by referring to Figure 3-4. The bold line indicates the basic power handling portion of the circuit. Transistors Q_1 and Q_2 together are alternately turned ON for a period of time ΔT_1 and OFF for a period ΔT_2. During ΔT_1, the input (line) voltage is impressed across windings N_p of transformer T_2 and N_1 of saturating transformer T_1. An increment of energy stored in the core causes the polarity of the voltage across N_s and N_p suddenly to

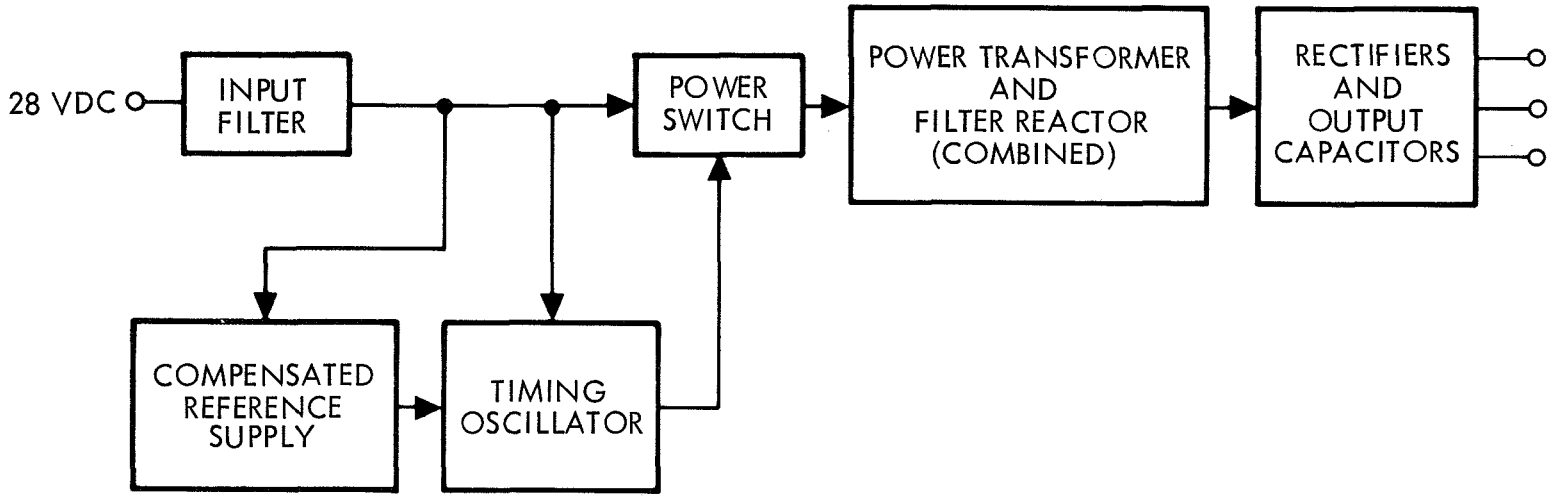


Figure 3-2. Power Converter MPC1 Block Diagram

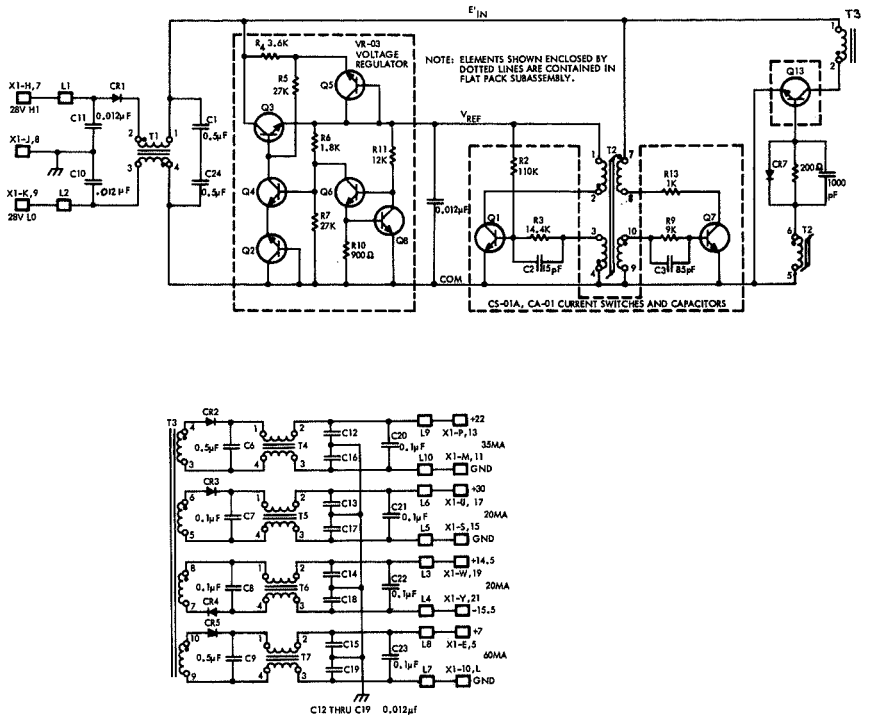


Figure 3-3. Power Converter MPC-2 Schematic

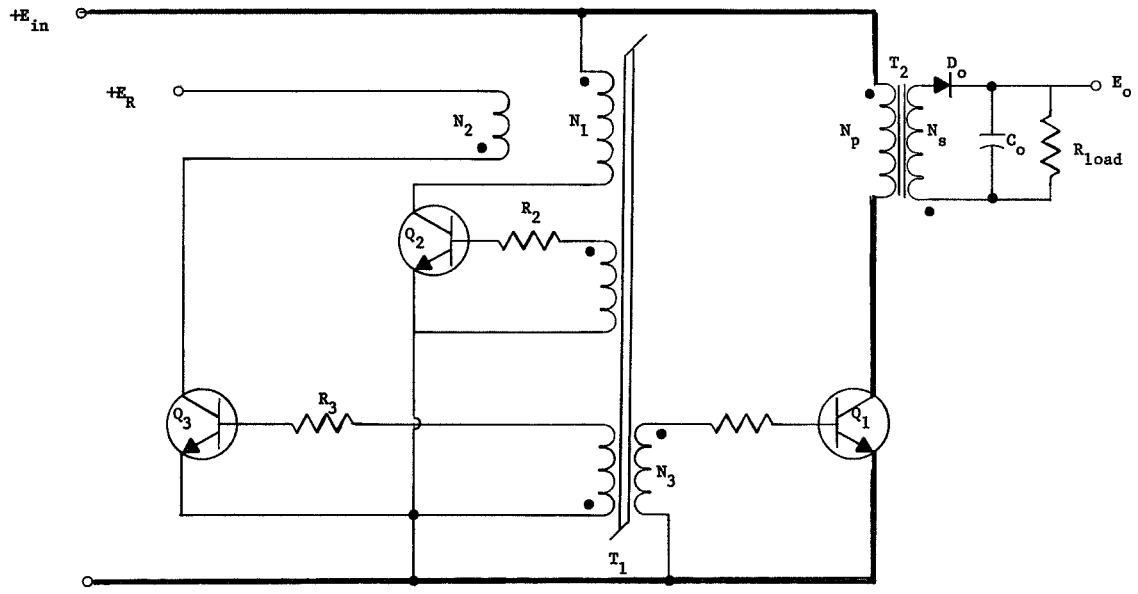


Figure 3-4. Basic Converter Circuit Schematic

reverse. The reversed polarity across N_p causes a current flow through diode D_o into capacitor C_o and the load. The rate at which power is delivered to the load is related to the ratio $\Delta T_1/\Delta T_2$ of power switch Q_1; by controlling this ratio, the output voltage, E_o, can be regulated.

The circuit, consisting of transistors Q_2 and Q_3, transformer T_1, and resistors R_2 and R_3, comprises a standard magnetically-coupled square wave oscillator. The alternate half cycles of oscillation are not necessarily equal. The period ΔT_2, during which Q_3 conducts (and Q_2 and Q_1 are OFF), is determined by a fixed reference voltage, E_R. In this manner the output voltage can, in principle, be made independent of input voltage. This is shown in the following equations which assume ideal circuit components.

For transformer T_1

$$\Delta T_1 = \frac{2\phi_s N_1}{E_{in} \times 10^8} \quad \text{(where } \phi_s \text{ is saturation flux)} \tag{3-1}$$

$$\Delta T_2 = \frac{2\phi_s N_2}{E_R \times 10^8} \tag{3-2}$$

For transformer T_2

$$\Delta T_1 = \frac{\Delta\phi N_p}{E_{in} \times 10^8} \quad \text{(where } \Delta\phi \text{ is the steady state flux change in } T_2\text{)} \tag{3-3}$$

$$\Delta T_2 = \frac{\Delta\phi N_s}{E_o 10^8} \tag{3-4}$$

Combining these equations yields

$$E_o = \left(\frac{N_1}{N_2}\right)\left(\frac{N_s}{N_p}\right)E_R \qquad \text{NOTE: } E_o \text{ is independent of } E_{in}. \qquad (3\text{-}5)$$

Thus, as line voltage increases, the ratio $\Delta T_1/\Delta T_2$ changes in such a manner so as to keep the output voltage constant. ΔT_2 is fixed and ΔT_1, which establishes the variable ON time of Q_1, varies directly with input voltage. Switching frequency hence varies, being a minimum at low line.

The circuit shown previously in Figure 3-3 was designed to operate at approximately 200 Hz at low line (22 vdc). The reference voltage, which establishes time ΔT_2, is provided by a low-level series regulator consisting of transistors Q_4 and Q_3, zener references Q_2 and Q_5, and associated resistors. Because of nonideal components which can result in unequal volt-second products applied to cores T_1 and T_2, the regulation characteristic of the basic converter exhibits a small positive increase in the output with increasing input line voltage. One reason is the change in storage time of Q_{13} under varying line conditions. The additional circuitry within the referenced supply, consisting of transistors Q_6 and Q_8, and resistors R_{10} and R_{11}, provides a means of temperature compensation. Adjustment of R_{10} establishes the desired temperature characteristic.

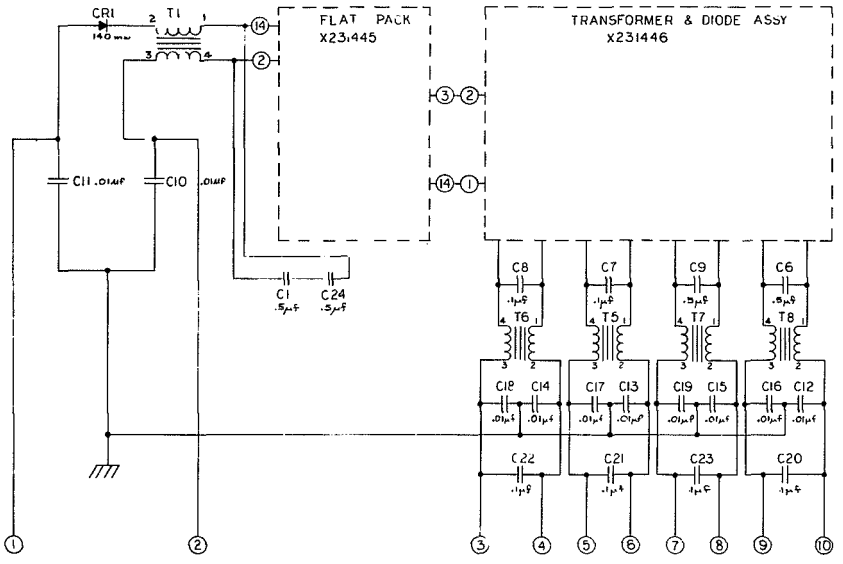
The tuning oscillator which provides the variable drive pulse to power switch Q_{13} is of standard design. A starting resistor, R_2, at the base of Q_1, establishes reliable starting at all temperature conditions. The reference supply and the timing oscillator consist of integrated circuit devices. The timing core is 1/8-mil Permalloy. Because of the required power level of 3 watts, a discrete component transistor is used for the power switch.

The output transformer (and filter reactor) is of the powder Mo-Permalloy type having a permeability of 160. The output rectifiers are blocked during the ON time of Q_1 (ΔT_1). The output capacitors deliver energy to the load during this variable period. During the time ΔT_2, the output transformer delivers energy to the load and recharges the filter capacitors. Ripple voltage is primarily a function of output capacitance and load. Microminiature ceramic capacitors and filter chokes are used for filtering. The rectifier connections shown in Figure 3-3 provide plus and minus output levels to the transducer and dc amplifier regulator circuits.

The input filter, T_1, C_1, C_{10}, C_{11}, and C_{24}, limit the amount of ripple fed back into the source. T_1 is wound with special resistance wire in order to dampen the filter response at its resonant frequency. Diode CR_1 provides reverse polarity protection for the converter.

Efficiency of the overall unit is about 70 percent at an input of 28 vdc. Converter components are designed and/or rated to sustain a maximum transient input voltage level of 50 V. The input filter inductor T_1 is the largest component in the system. Its size is dictated by the transient susceptibility requirements.

Figures 3-5 and 3-6 show the physical layout of the Model MPC-1 Converter. Figure 3-5 shows the converter with the cover attached in isometric form and also the electrical interconnections between the three basic subassemblies. These are the passive components, flat pack assembly, and transformer and diode assembly, as shown in Figure 3-7. Figure 3-6 is an overall layout of the converter and shows the physical interconnections between the basic components and the printed circuit board. The printed circuit board is used to perform the majority of interconnections. The printer interconnecting paths are shown as crosshatched areas on the layout drawing.



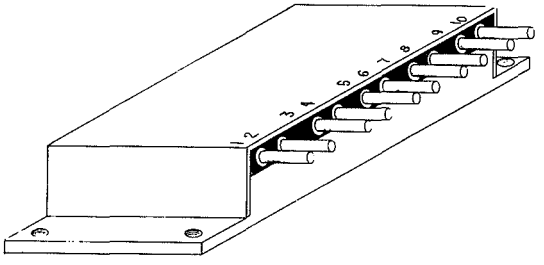


Figure 3-5. Power Converter Subassembly Drawing

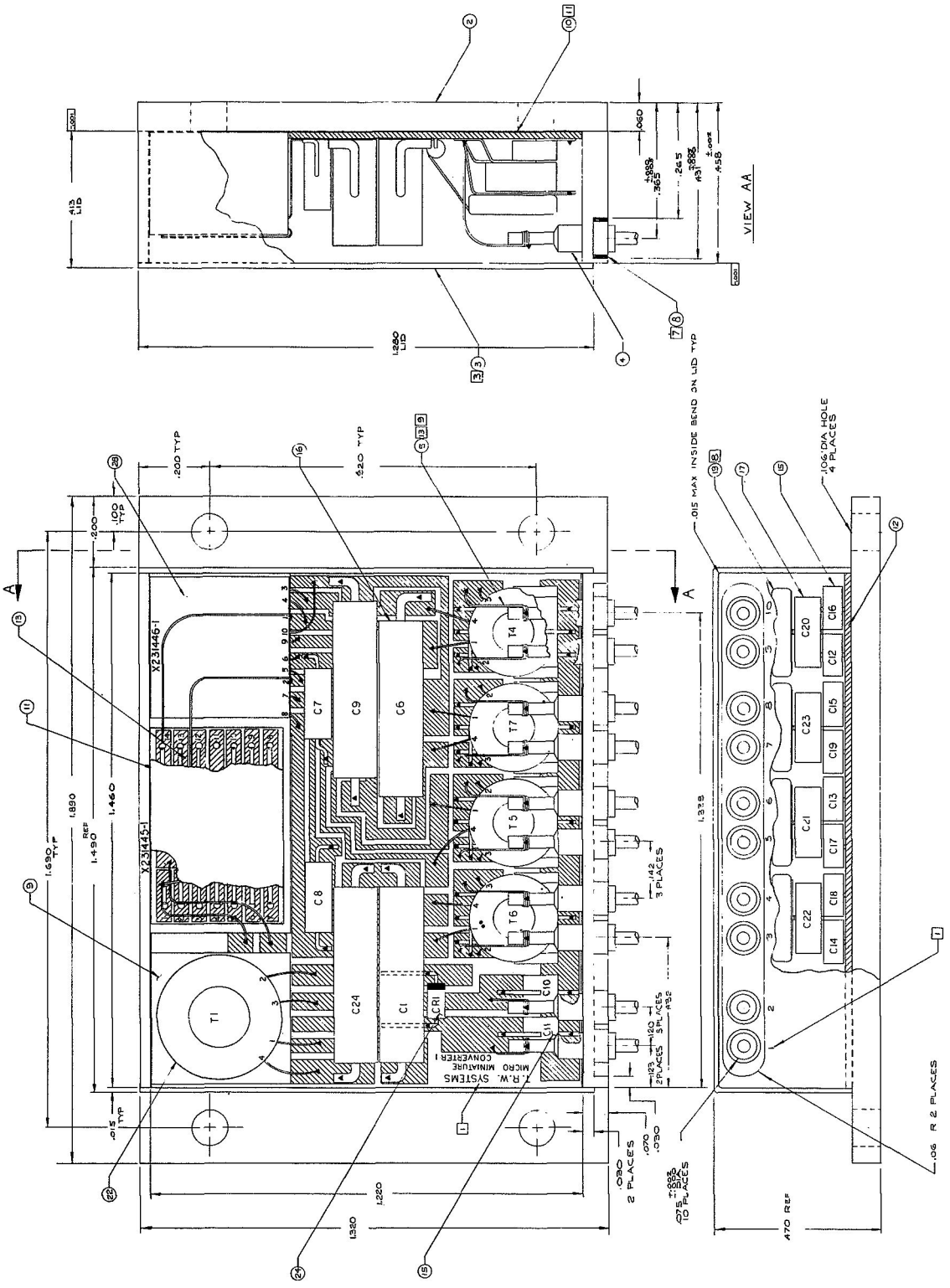


Figure 3-6. Power Converter Main Assembly Drawing

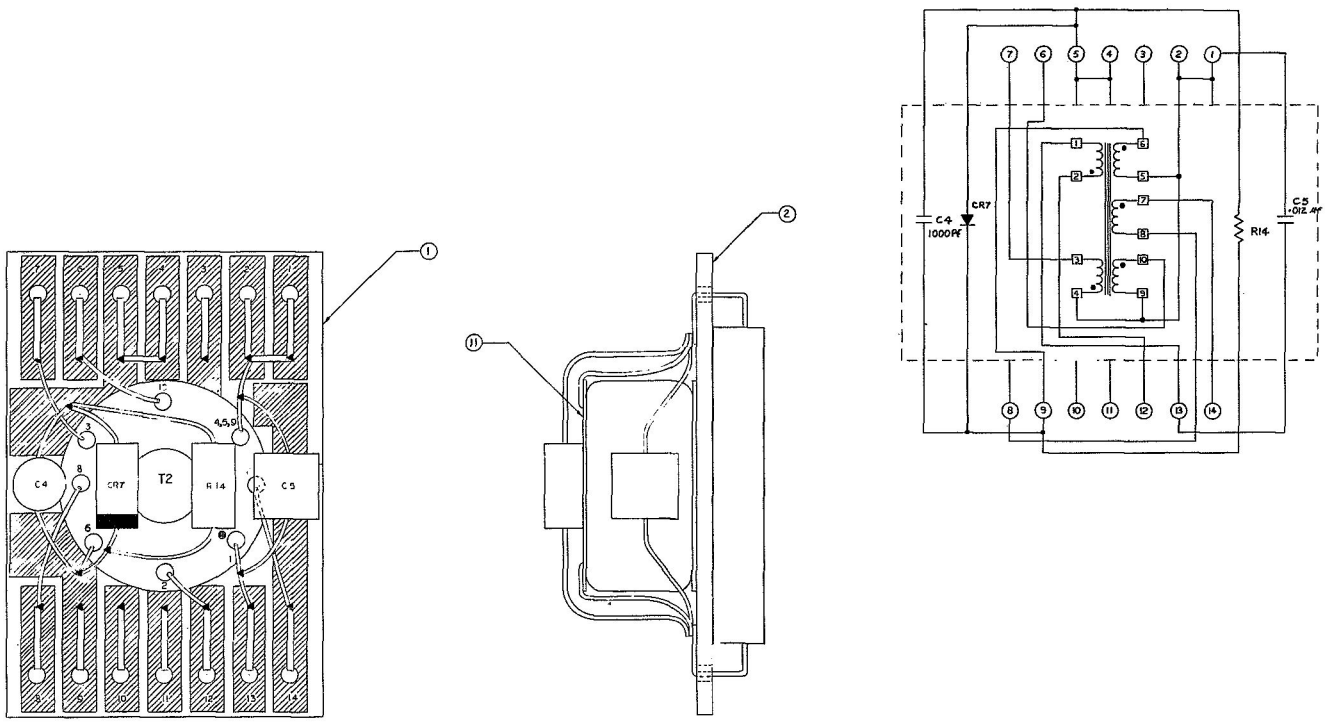


Figure 3-7. Power Converter Flat Pack Lid Assembly

Figure 3-7 is a detailed layout of the flat pack lid assembly located at the top center of the converter package, as shown in Figure 3-6. It shows the printed circuit board with the assembled transformer T_2. T_2 is the timing transformer used in the magnetically coupled square wave oscillator. Mounted on top of T_2 are two discrete ceramic capacitors, C_4 and C_5, and resistor R_{14} and diode CR_7. CR, R_{14}, and CR_7 are wired in parallel to form the base drive circuit for the power output transistor Q_{13}.

Figure 3-8 shows a top view of the 3/8 x 3/8 inch flat pack used to mount the active components of the converter. It contains output transistor Q_{13} and three integrated circuit chips. The first chip, CS-01A, consists of transistors and resistors used to make up the current switch portion of the converter. The second chip, CA-01, consists of MOS-type capacitors, C_2 and C_3. The third chip, VR-03, is the voltage regulator used to supply V_{REF} to the current switch transistor Q_1. The black lines shown interconnecting the three integrated circuit chips and power transistor Q_{13} are gold wires. The collector of Q_{13} is connected directly to an isolated pad inside the package, as shown by the drawing. Note that the other three chips all use a common mounting pad. This pad is connected to the COM connection of the flat pack, pins 1 and 2.

Figures 3-9 and 3-10, respectively, show the electrical schematic and integrated circuit assembly of the Voltage Regulator VR03. Dimensions on the sides of the physical layout indicate overall size in thousandths of an inch. As per the discussion on voltage regulator adjustment, resistor R_6, R_{10}, R_{11}, R_7, and R_4 are made adjustable by either blowing out the normally shorted fuse links, or shorting out the normally open lines by applying a ball bond over the specially made pad areas.

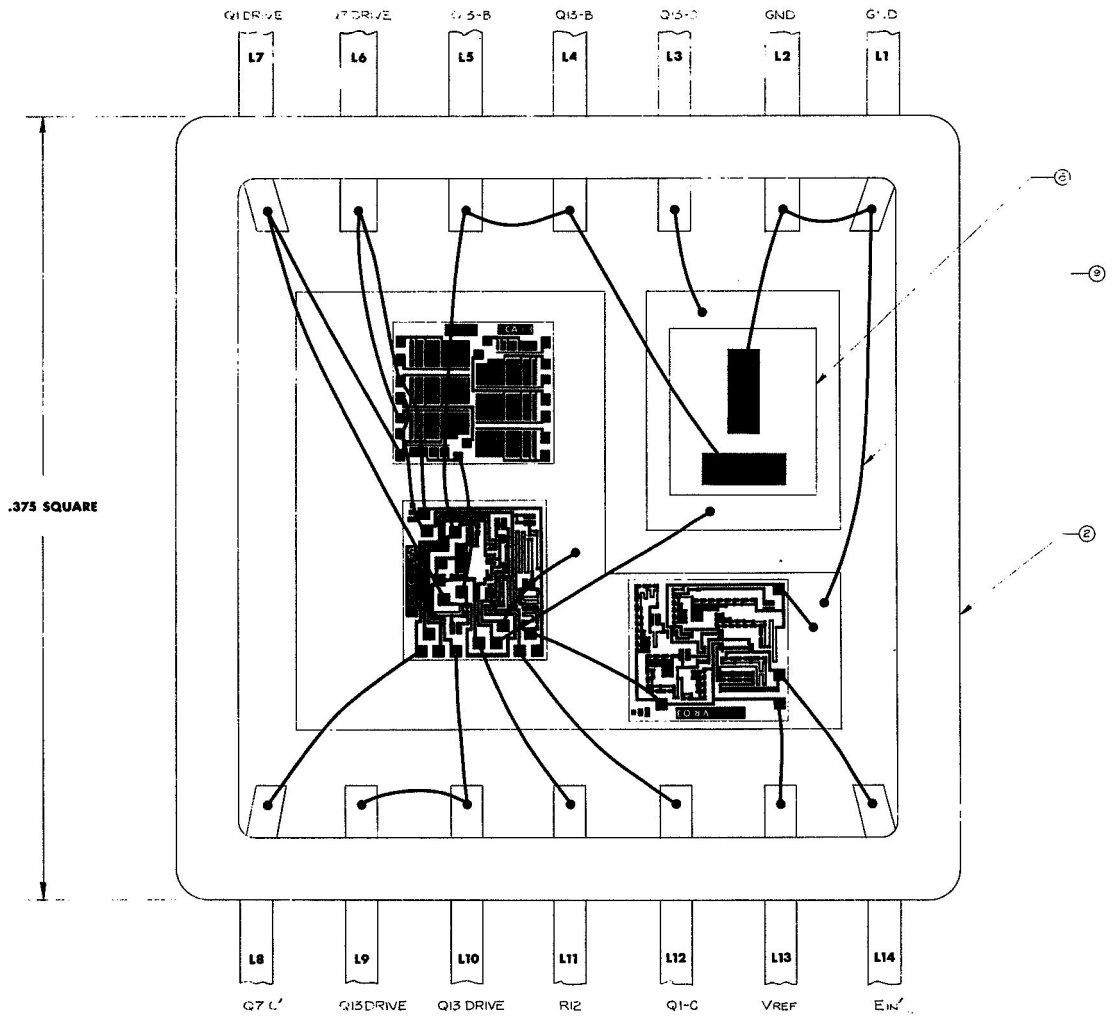


Figure 3-8. Power Converter Flat Pack
Internal Wiring

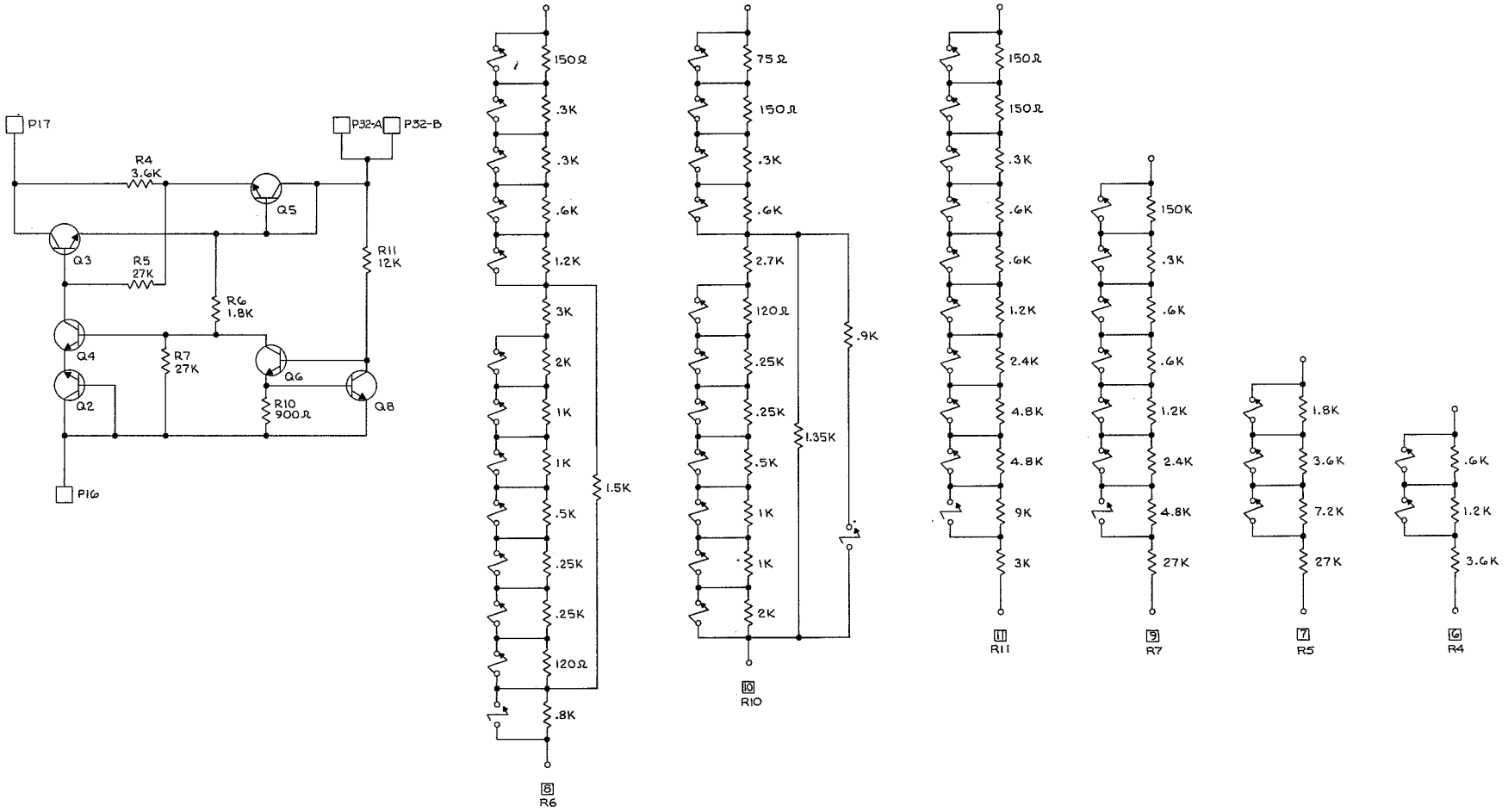


Figure 3-9. Voltage Regulator (VR03) Schematic

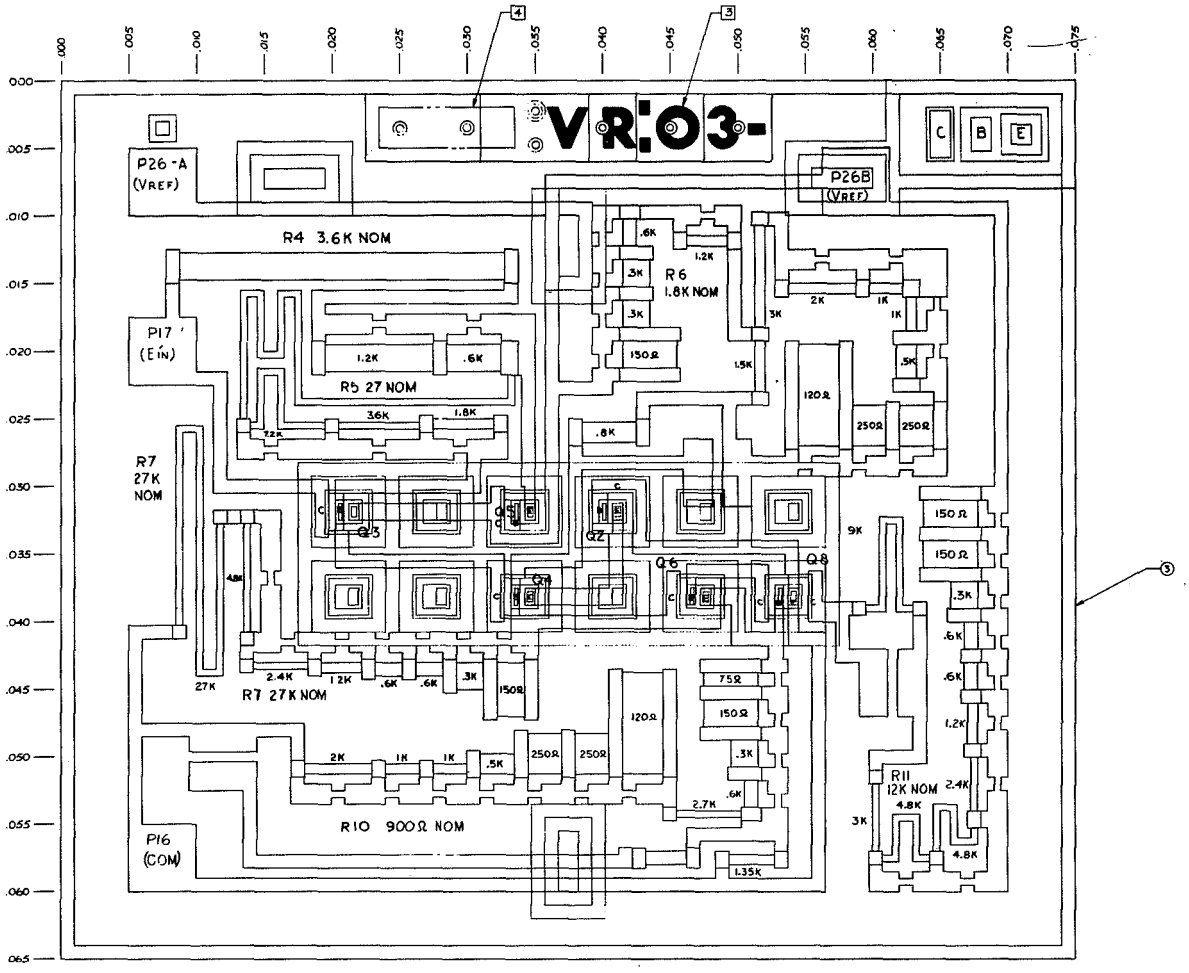


Figure 3-10. Voltage Regulator (VR03) Assembly Drawing

Figures 3-11 and 3-12, respectively, show the electrical schematic and physical layout of the Converter Switch CS-01A. Resistors R_2, R_3, R_9, and R_{13} are made adjustable over a range of $\pm$ 10 percent. This is accomplished by either blowing out the normally shorted fuse links or shorting out the normally open links, in the same manner as mentioned for the VR03 circuit. Note that although transistors Q_{12}, Q_{14}, Q_{15}, and Q_{16}, and resistor R_{12} are on the chip, they are not used in the converter circuit design.

The following photographs are included:

Figure 3-13. Overall Package

Figure 3-14. Converter Test Board

Figure 3-15. Filter Subassembly

Figure 3-16. T_2 Assembly

Figure 3-17. Integrated Circuit Module

3.2.2 Summary of Measured Performance Data

The output of the microminiature power converter is measured as a function of temperature and input variations, with nominal loading, in Table 3-II.

TABLE 3-II

Serial No. 63		-35°C	0°C	+25°C	+95°C
V_1	V_{in} = 22	21.954	22.411	22.343	22.302
	= 28	23.185	23.373	23.367	23.128
	= 32	23.642	23.752	23.763	23.468
V_2	V_{in} = 22	22.061	22.494	22.423	22.355
	= 28	23.265	23.435	22.425	23.163
	= 32	23.707	23.802	23.810	23.498
V_3	V_{in} = 22	15.945	16.262	16.210	16.154
	= 28	16.857	16.979	16.967	16.771
	= 32	17.195	17.261	17.262	17.024

TABLE 3-II (Contd.)

		-35°C	0°C	+25°C	+95°C
Serial No. 965					
V_1	V_{in} = 22	21.834	21.750	21.682	21.266
	V_{in} = 28	23.217	23.053	22.833	22.473
	V_{in} = 32	23.912	23.701	23.474	23.097
V_2	V_{in} = 22	21.924	21.830	21.650	21.322
	V_{in} = 28	23.289	23.114	22.888	22.518
	V_{in} = 32	23.977	23.755	23.523	23.133
V_3	V_{in} = 22	15.813	15.736	15.595	15.358
	V_{in} = 28	16.830	16.690	16.517	16.256
	V_{in} = 32	17.338	16.165	16.987	16.718
Serial No. 966					
V_1	V_{in} = 22	22.860	22.870	22.781	22.492
	V_{in} = 28	23.675	23.551	23.468	23.130
	V_{in} = 32	24.113	23.935	23.881	23.598
V_2	V_{in} = 22	22.903	22.910	22.819	22.507
	V_{in} = 28	23.708	23.571	23.487	23.135
	V_{in} = 32	24.139	23.947	23.894	23.597
V_3	V_{in} = 22	16.593	16.595	16.525	16.298
	V_{in} = 28	17.197	17.090	17.028	16.775
	V_{in} = 32	17.518	17.373	17.334	17.121
Serial No. 968					
V_1	V_{in} = 22	22.765	22.865	22.846	22.635
	V_{in} = 28	23.253	23.357	23.344	23.197
	V_{in} = 32	23.502	23.613	23.606	23.483
V_2	V_{in} = 22	22.846	22.917	22.893	22.673
	V_{in} = 28	23.297	23.380	23.360	23.209
	V_{in} = 32	23.528	23.617	23.607	23.482
V_3	V_{in} = 22	16.520	16.572	16.552	16.390
	V_{in} = 28	16.873	16.931	16.915	16.803
	V_{in} = 32	17.053	17.115	17.106	17.010
Serial No. 967					
V_1	V_{in} = 22	23.166	23.153	23.076	23.004
	V_{in} = 28	23.689	23.686	23.624	23.638
	V_{in} = 32	23.992	23.992	23.992	23.893
V_2	V_{in} = 22	23.217	23.211	23.114	23.067
	V_{in} = 28	23.722	23.716	23.643	23.655
	V_{in} = 32	24.017	24.011	23.933	23.905
V_3	V_{in} = 22	16.817	16.813	16.745	16.678
	V_{in} = 28	17.208	17.205	17.152	17.153
	V_{in} = 32	17.432	17.430	17.373	17.343

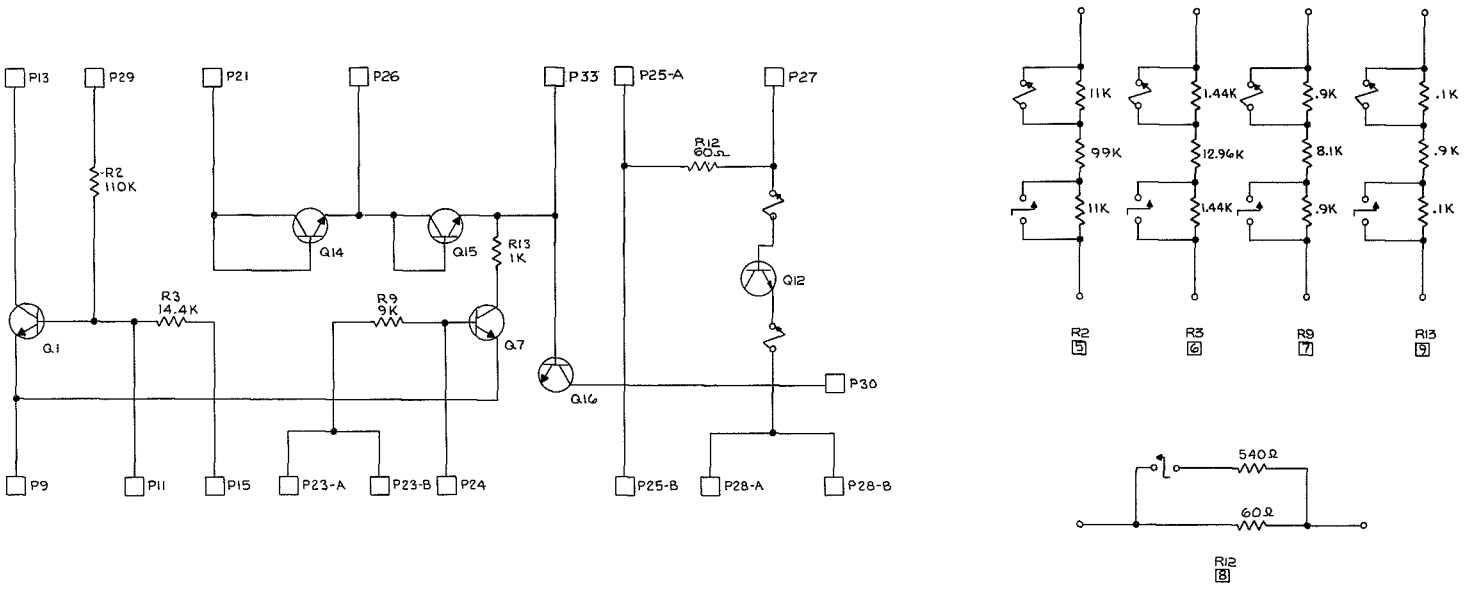


Figure 3-11. Converter Switch (CS01A) Schematic

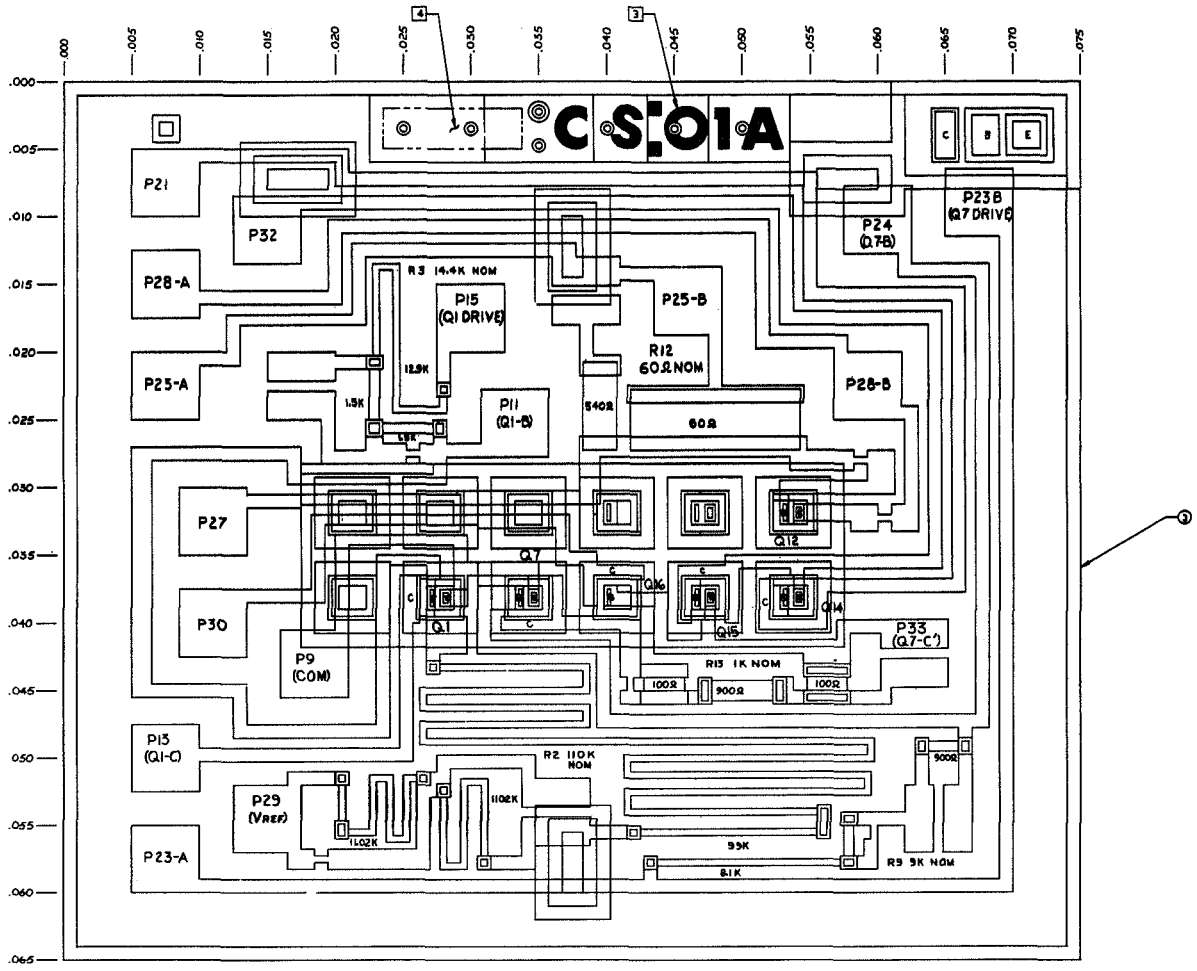


Figure 3-12. Converter Switch (CS01A) Assembly Drawing

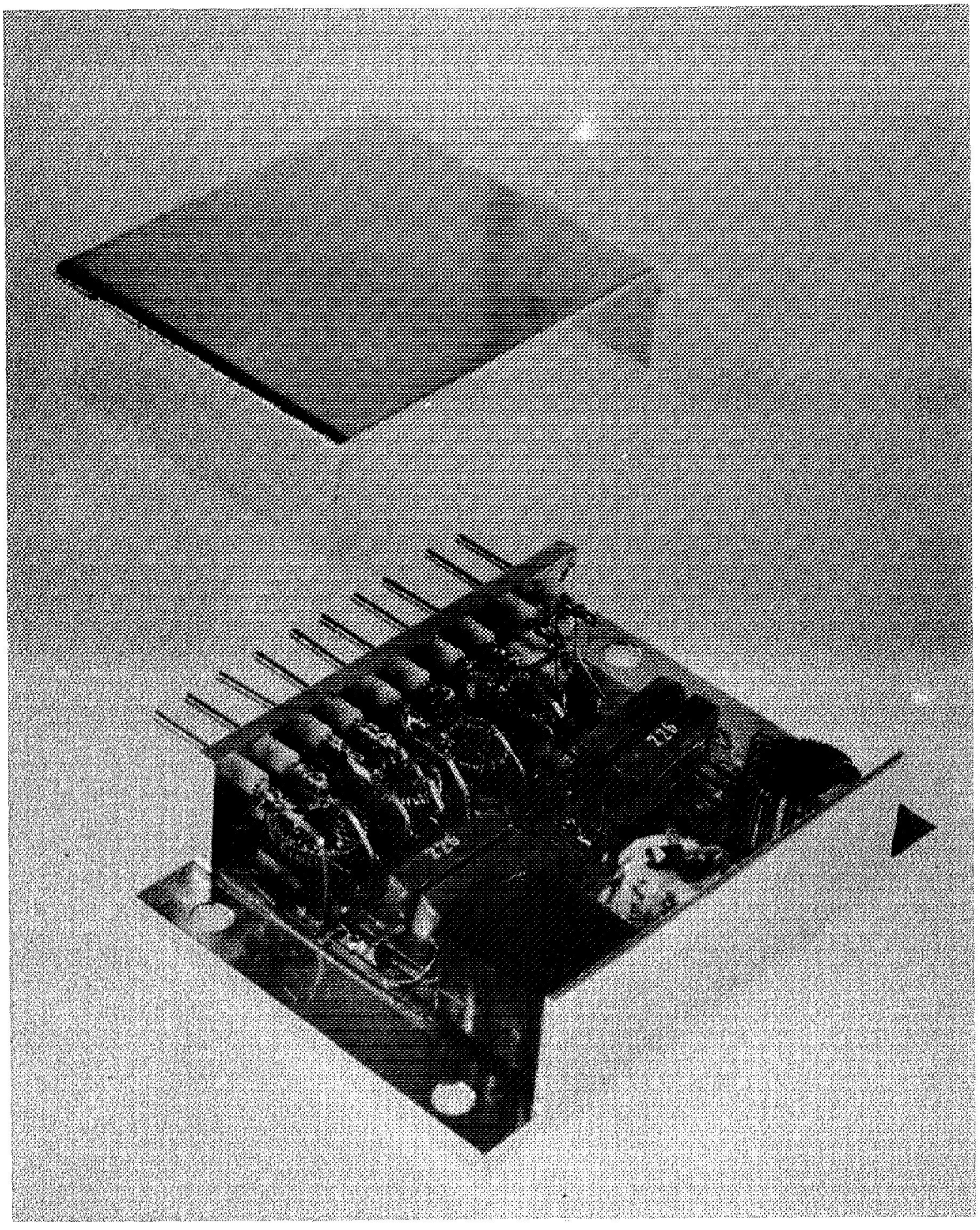


Figure 3-13. Converter Switch (CS01A) Overall Package

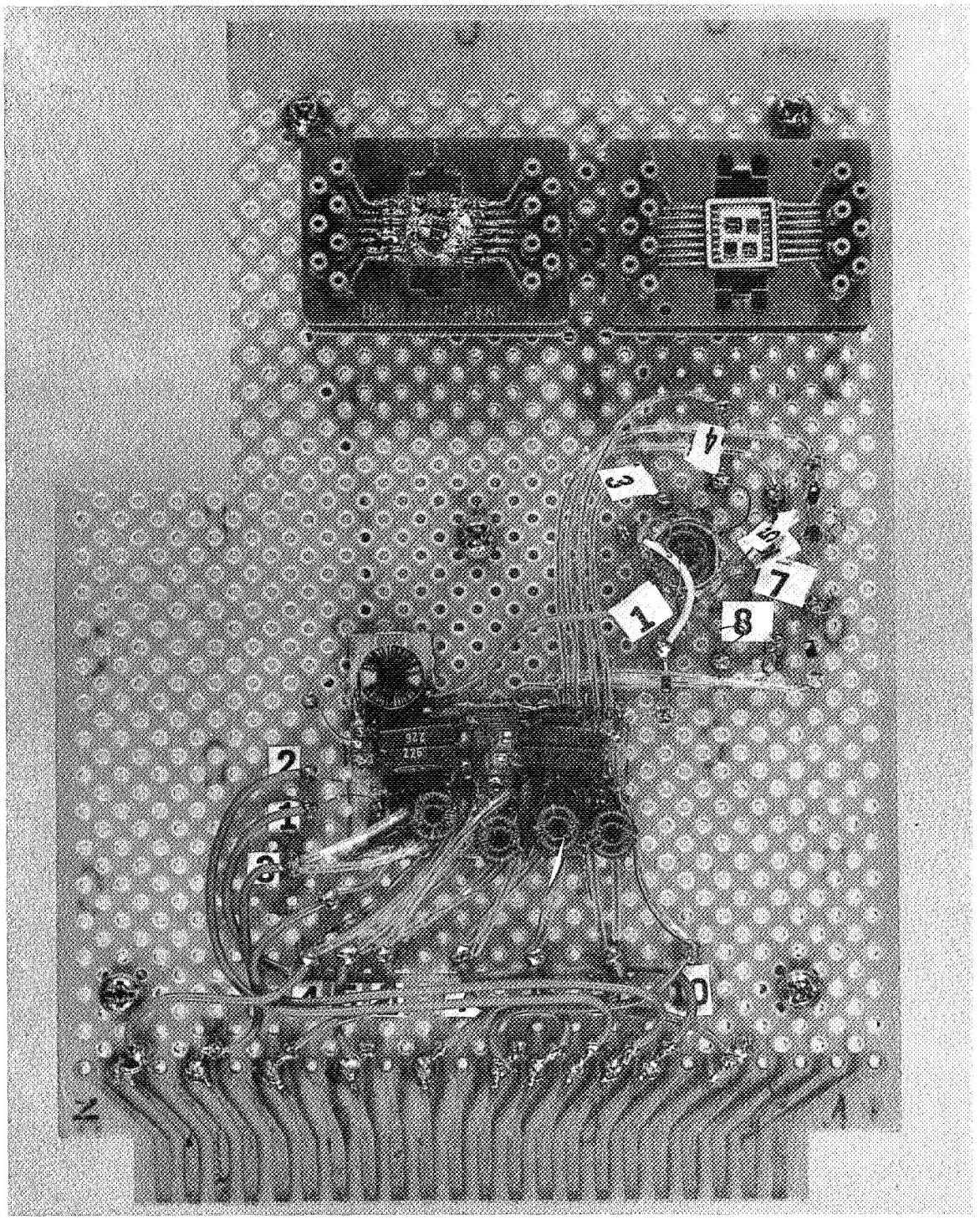


Figure 3-14. Converter Switch Test Board

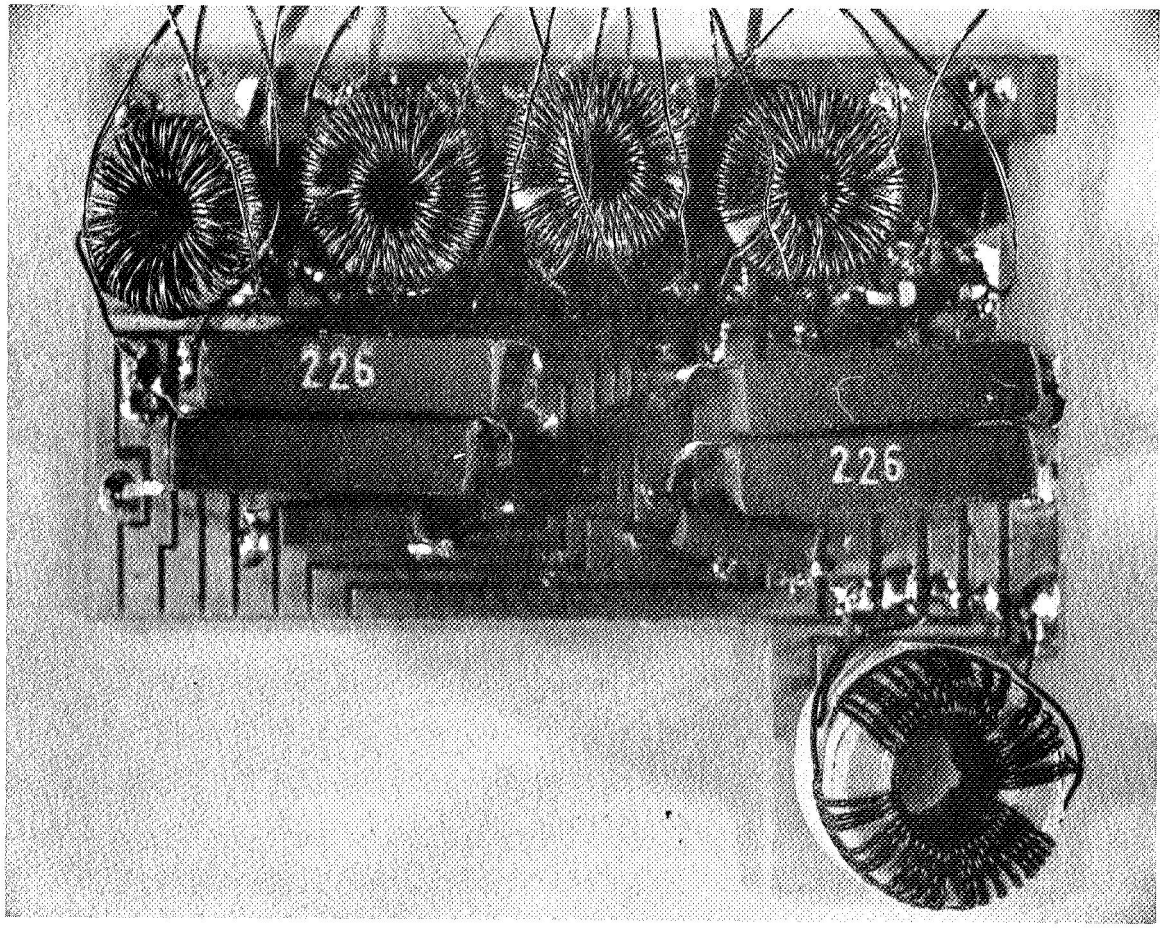


Figure 3-15. Converter Switch Filter Subassembly

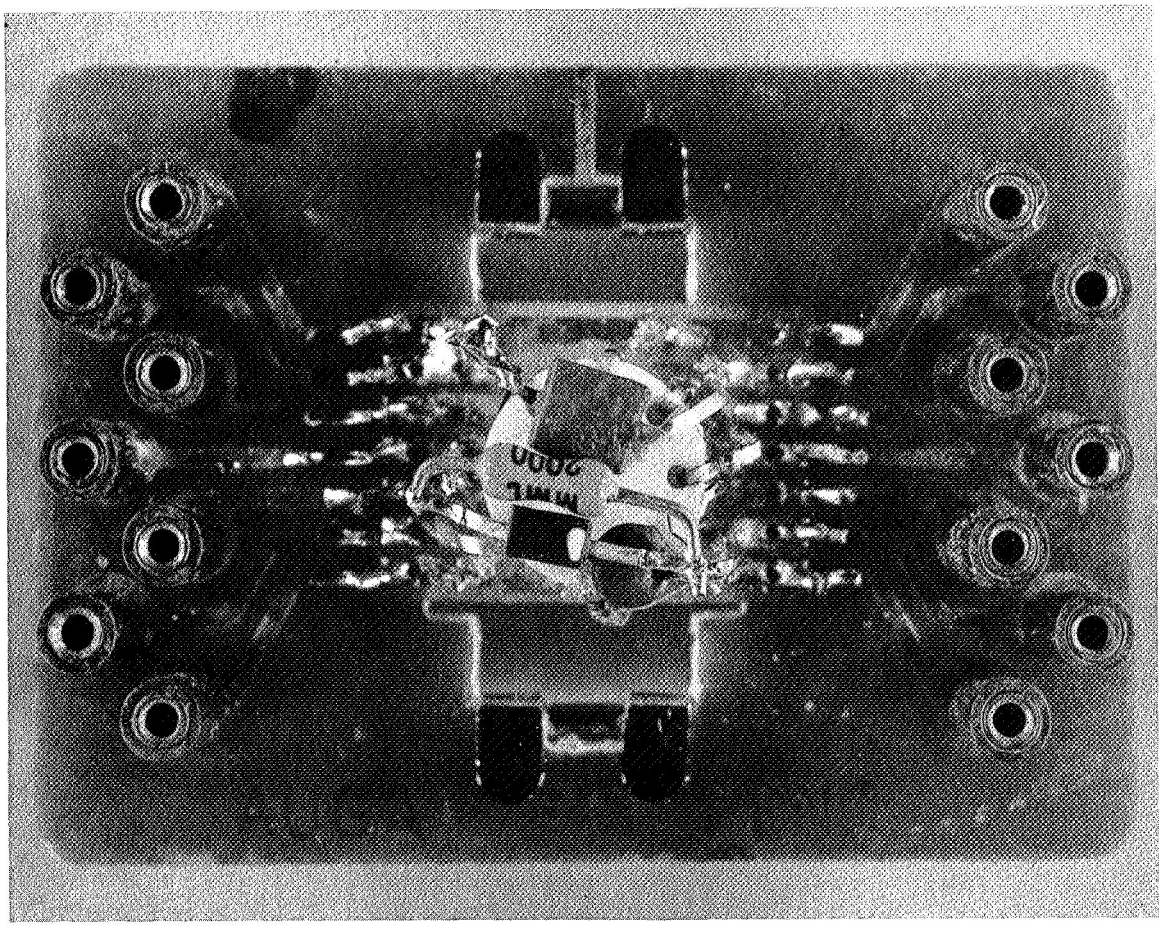


Figure 3-16. Converter Switch T2 Assembly

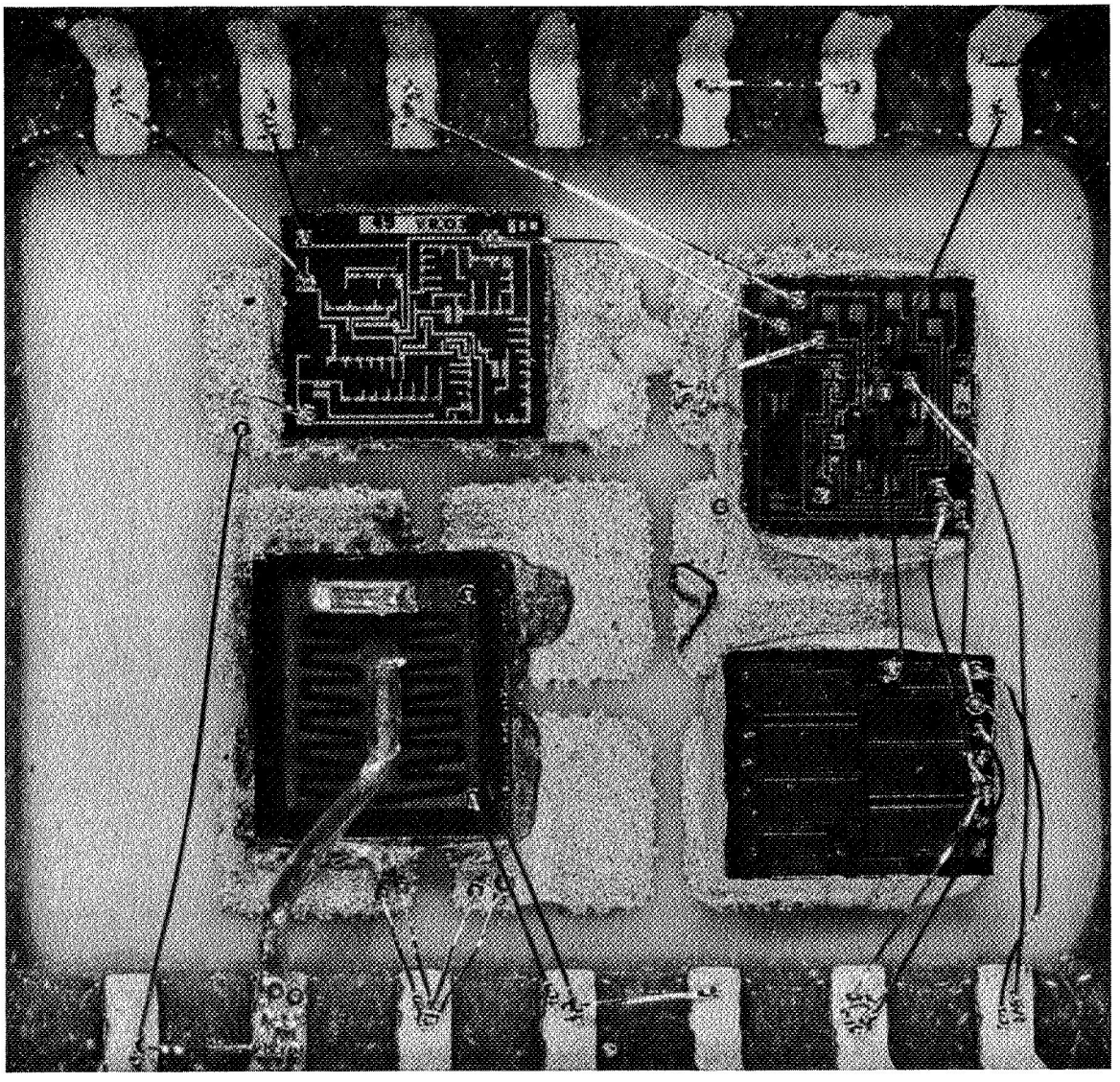


Figure 3-17. Converter Switch Integrated Circuit Module

3.3 REGULATORS

3.3.1 Design Principles

This section describes the circuit mechanization of the monolithic voltage regulators which follow the power converter. The following discussion applies to both the VR34 and VR35, since the organization of both circuits are similar. Figure 3-18 shows the general circuit approach used to meet the specifications.

Differential amplifier, A, maintains the junction of R_B and R_C at a reference voltage by controlling the base voltage of Q_A. Conventional regulators use a resistor from the base of the series regulating element, Q_A, to the positive supply potential, V_1. Instead, a preregulated PNP-current generator replaces this resistor for the following reasons:

a) For given bias conditions, the dynamic collector impedance of the current generator is considerably larger than a conventionally used resistor. The feedback loop gain, which is directly proportional to this impedance, is therefore increased.

b) The preregulation aspect of this current generator further isolates the remaining circuit from the effects of input line voltage variations, thereby increasing the line regulation.

Figure 3-19(a) shows the preregulated PNP-current generator. The output current is controlled by the voltage across R_D, which is approximately equal to the voltage across R_E. The forward biased emitter-base junction of Q_D is used for temperature stabilization. The reverse emitter-base breakdown voltage of Q_E stabilizes the voltage across R_E and R_F, and therefore regulates the output current against changes in input line voltage.

A lateral geometry, side-injection PNP transistor is used in the monolithic integrated regulator circuit because of the relative ease in fabricating the device in the same substrate with NPN transistors. However,

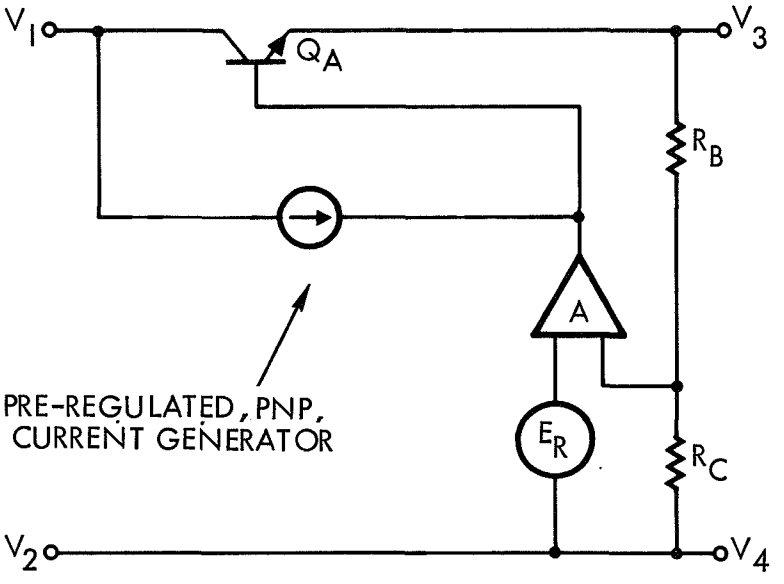


Figure 3-18. Gated Regulator Circuit Organization

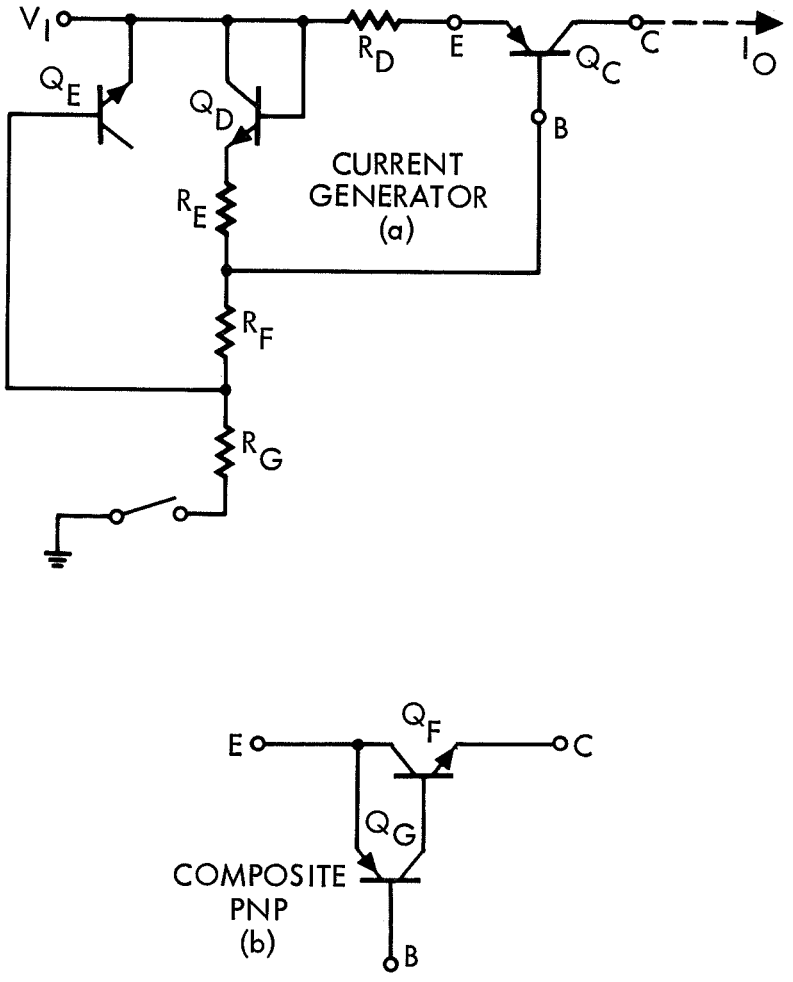


Figure 3-19. Regulator Current Generator Schematic

the disadvantages of such a structure include low current gains ($\beta = 1 - 5$) and poor frequency response. Therefore, the composite structure shown in Figure 3-19(b) is used in place of Q_C because the effective β of the pair is the product of the β's of Q_F and Q_G.

The fabrication of the side-injection PNP transistor with buried layer epitaxial techniques presents difficulties in maintaining low substrate leakage currents and low substrate parasitic PNP β's. To circumvent these problems, the dielectric isolation process was selected as the appropriate technique for regulator substrate fabrication. A common substrate type (MCD3) is used for all regulators. Each regulator circuit type is fabricated by applying unique resistor and interconnect masks to the dielectrically isolated MCD3 substrate.

The VR34 schematic is shown in Figure 3-20. This same integrated circuit is used as a gated regulator, so it includes extra circuit components which are not used in the nongated case.

Transistor Q_1 monitors the voltage across the resistor R_5. Q_1 is normally off, but during an overcurrent condition, Q_1 will start to turn on, thereby turning off the current generator. This limits the short circuit current to a value approximately double the nominal current level.

Resistor R_{11} is included in the composite PNP structure (Q_6 and Q_7) to minimize the turn-off time in the gated application. Transistor structures Q_8 and Q_9 are used as roll-off capacitors to dynamically stabilize the closed loop feedback circuit. Emitter follower, Q_{12}, drives the series regulating transistor, Q_{13}. R_{13} is connected to the emitter of Q_{12} to stabilize and increase the operating current of Q_{12}.

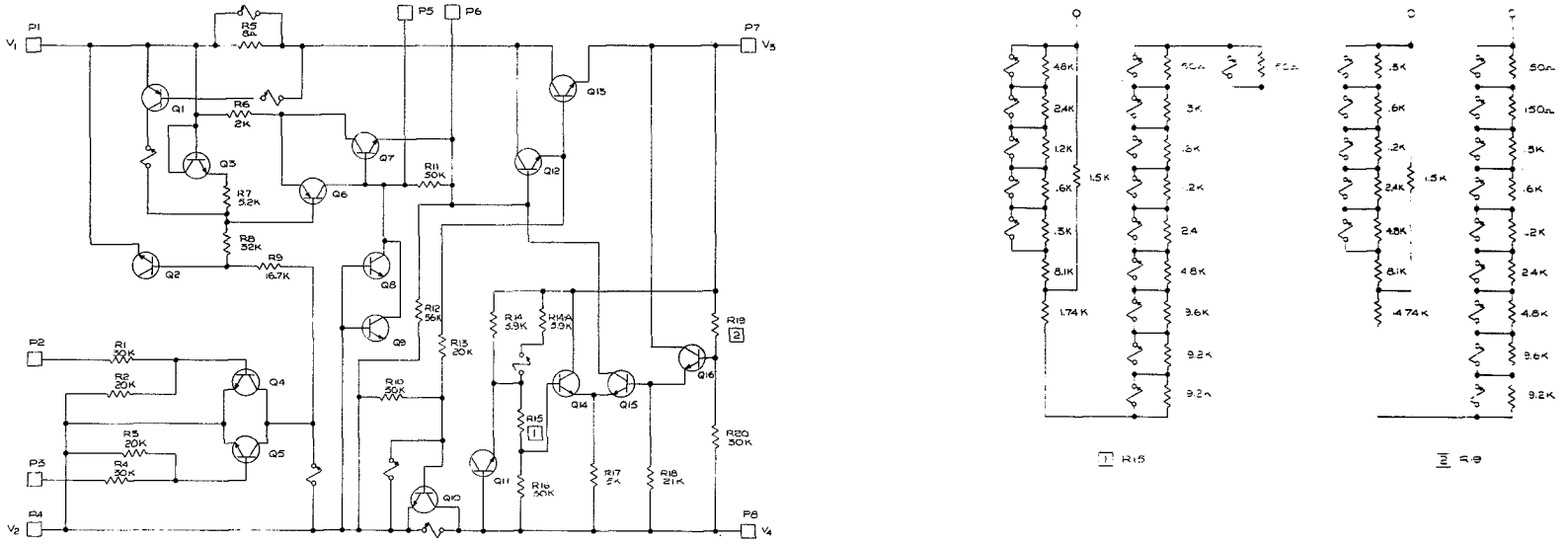


Figure 3-20. VR34 Schematic

The emitter-base junction of Q_{11} is reverse biased and used as a voltage reference diode. The typical parameter distributions are

$$BV_{BEO} = 6.5 \text{ to } 9.5 \text{ volts} \tag{3-6}$$

$$\frac{\partial BV_{BEO}}{\partial T} = 3 \text{ to } 5 \frac{mV}{^{o}C} \tag{3-7}$$

Resistive divider, R_{15} and R_{16}, is adjusted to develop a voltage temperature coefficient at the base of Q_{14} which is exactly equal and opposite to the temperature coefficient of the forward-biased emitter-base junction of Q_{16}. This establishes the base voltage of Q_{16} constant with respect to temperature. The regulator output voltage is then adjusted precisely to 10.00 volts by increasing R_{19}. This procedure allows the output voltage temperature drift and offset to be independently selected, thereby simplifying the adjustment procedure.

Table 3-II indicates typical performance data for the VR34. The temperature performance is limited only by the nonlinearities and resolution of the resistor adjustments. The circuit was designed to drive either a 350 ohm or a 175 ohm transducer. For the latter case, care must be given to the package thermal characteristics to insure proper performance at +95°C.

Figure 3-21 shows the assembly drawing of the VR34 integrated circuit which incorporates the dielectrically isolated MCD3 substrate.

Q_{10} and Q_{13} are large geometry NPN transistors designed to accommodate the 60 mA load current demanded by the 175 ohm transducers. The lateral geometry of the three types of transistor structures are described in Section 6. The cermet resistor line widths are typically 0.6 mil with 0.8 mil spacing. The metal line widths are 1 mil.

TABLE 3-II. VR34 CHARACTERISTICS

Power	30 mA Load	60 mA Load
P_D (dissipated)	215 mW	395 mW
P_O (output)	300 mW	600 mW
P_I (input)	515 mW	995 mW
ξ (efficiency)	58%	60%
	$\frac{\partial V_O}{\partial V_I} \leq 2 \frac{mV}{volt}$	
	$\frac{\partial V_O}{\partial T} \leq 300 \frac{\mu V}{^oC}$	
	$\frac{\partial V_O}{\partial I_i} \leq 200 \frac{\mu V}{mA}$	

The VR35 schematic is shown in Figure 3-22. This circuit operates according to the VR34 description.

Table 3-III indicates typical performance data for the VR35.

Figure 3-23 shows the assembly drawing of the VR35 integrated circuit which also incorporates the dielectrically isolated MCD3 substrate with evaporated resistors and aluminum interconnect.

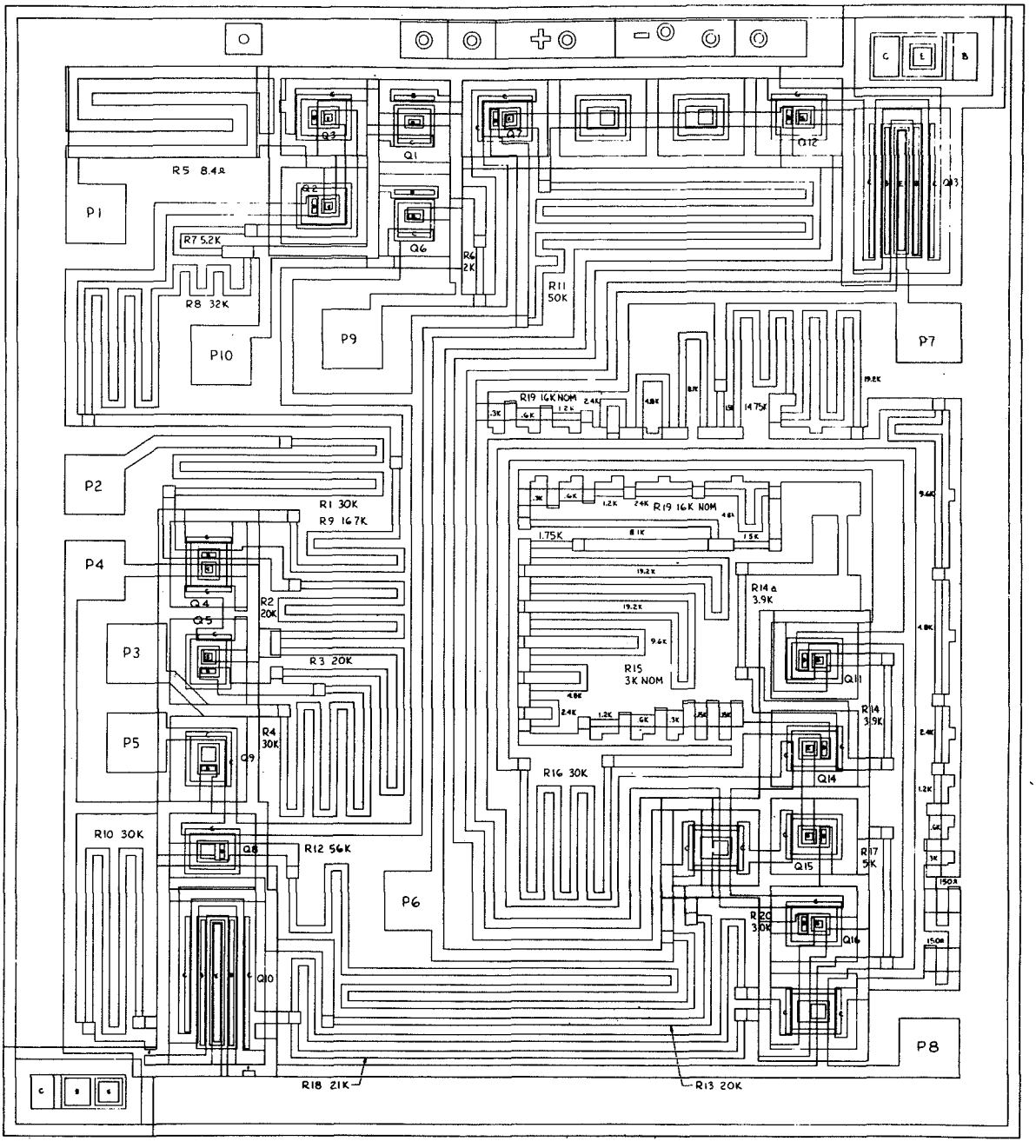


Figure 3-21. VR34 Assembly Drawing

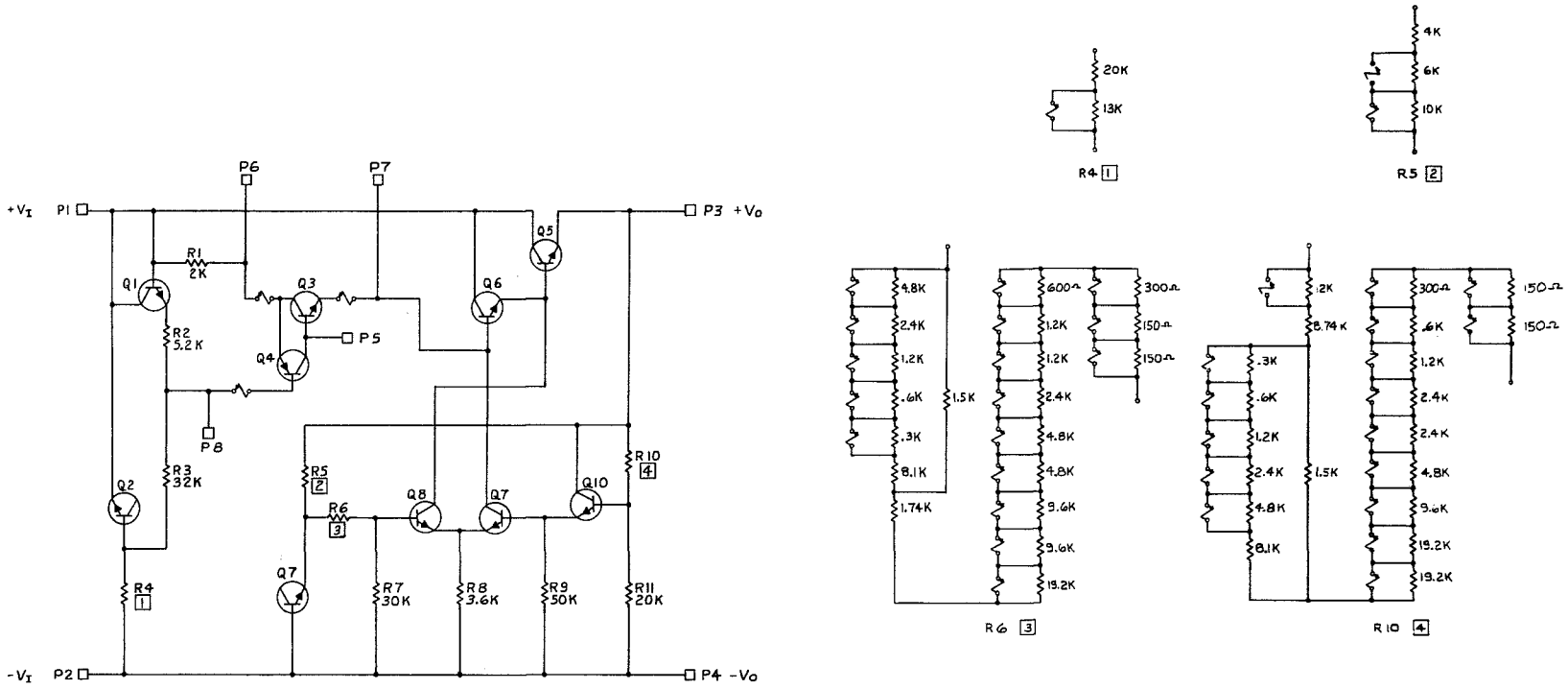


Figure 3-22. VR35 Schematic

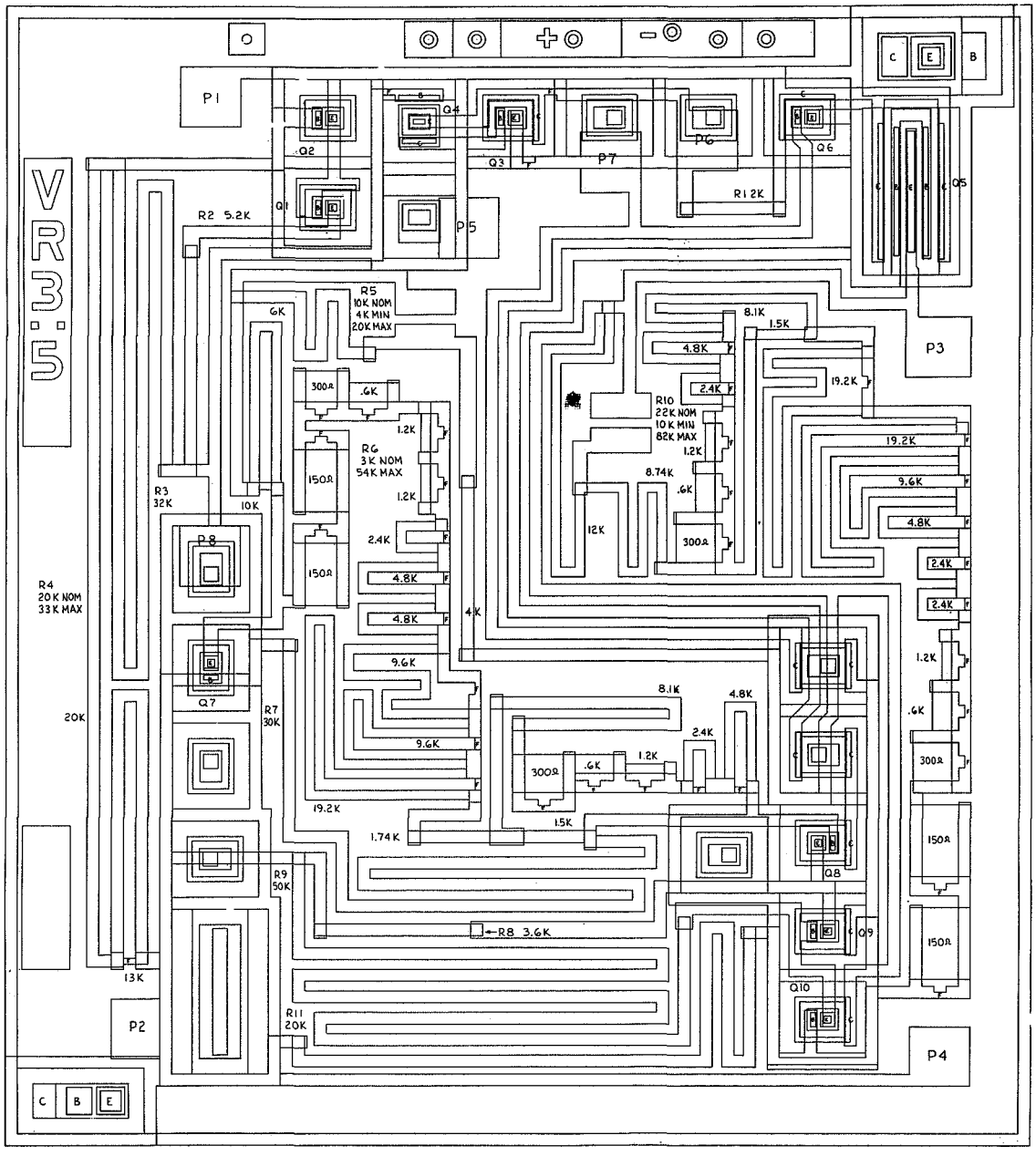


Figure 3-23. VR35 Assembly Drawing

TABLE 3-III. VR35 CHARACTERISTICS

P_D (dissipated) - 110 mW

P_O (output) - 90 mW

P_I (input) - 200 mW

ξ (efficiency) - 45%

$$\frac{\partial V_O}{\partial V_I} \leq 3 \frac{mV}{volt}$$

$$\frac{\partial V_O}{\partial T} \leq 1.5 \frac{mV*}{^oC}$$

$$\frac{\partial V_O}{\partial I_i} \leq 1 \frac{mV}{mA}$$

*This number can be reduced to 500 $\frac{\mu V}{^oC}$ or better by further adjustment.

4. INTEGRATED CIRCUIT TECHNIQUES

4.1 PROCESSING

Table 4-I designates the type of processing used in each of the integrated circuit modules developed by TRW Systems. Items 1 through 8 were developed and delivered under Contract No. NAS9-4640.

TABLE 4-I. PROCESSING TECHNIQUES USED IN TRW INTEGRATED CIRCUIT MODULES

Item	Name		Substrate	BLE	DI	MOS	CR
1	SCA41	Signal Modifier	MCD3	X			X
2	SCA42		MCD4	X			X
3	CAP		CA01			X	
4	VR34		MCD3		X		
5	VR35		MCD3		X		
6	CS01A	Power Converter	MCD1	X			X
7	VR03		MDC1	X			X
8	CA01		CA01			X	

where

BLE ≡ Buried Layer Epitaxy
DI ≡ Dielectric Isolation
MOS ≡ Metal-Oxide-Silicon
CR ≡ Cermet (evaporated) Resistors

4.1.1 Buried Layer Epitaxial Bipolar Transistors

Figure 4-1 shows a buried layer epitaxial bipolar transistor in cross section.

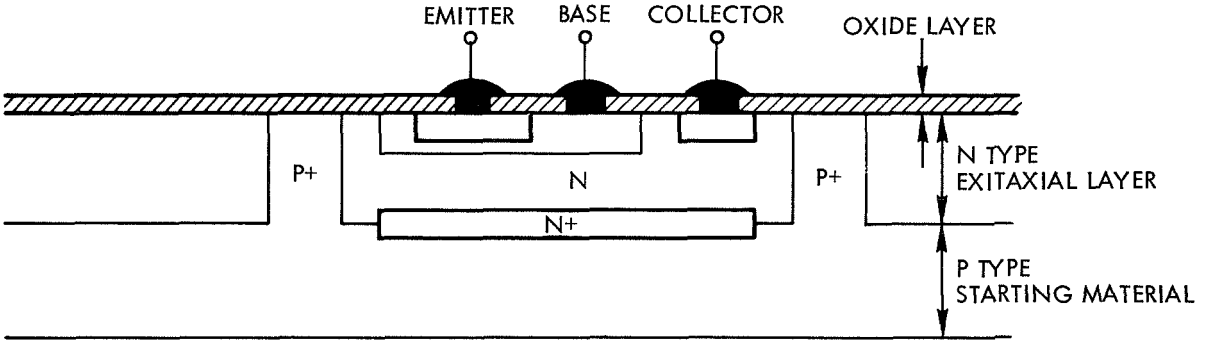


Figure 4-1. Cross Section of Buried Layer Epitaxial Transistors

The buried layer epitaxial processing technique is standard for TRW Systems and has the following sequence (Note the numerical values given were used in fabricating the MCD1.

1.	Starting Material	3.0 ± 5Ωcm P-type <100>
2.	Initial Oxidation	6-1/2F SiO_2 (sodium light; ≈ 13,000 Å thick)
3.	Photoresist Buried Layer N+	(Creates step in surface for post epitaxy identification)
4.	Oxidation	6-1/2F SiO_2
5.	Photoresist Buried Layer N+	(To expose areas for buried layer N+ collector diffusion)
6.	Buried Layer N+ Diffusion	Sb, monitor wafer 3Ωcm P-type sheet resistance 18Ω/□, depth 3.5μ
7.	Epitaxy	0.60 ± 0.15Ωcm; 10 ± 2μ, N-type
8.	Ethyl Silicate Oxide	6 ± 1/2 F SiO_2

9.	Photoresist Isolation Pattern (P+)	To Provide electrical isolated areas
10.	Gate Isolation Diffusion	N-propyl borate, sheet resistance 5Ω/□, depth 15μ
11.	Photoresist Base	To expose base areas
12.	Electrical Isolation Test	To insure electrical isolation, <1μa leakage at 30V
13.	Base Diffusion	B_2O_3, sheet resistance 160Ω/□, depth 3.0μ ≈ 9000 Å SiO_2 grown during diffusion
14.	Photoresist Emitter	To expose emitter areas
15.	Emitter Diffusion	P_2O_5, sheet resistance 3.5Ω/□, depth 1.35 ± 15
16.	Final Oxide	16,000 Å
17.	Photoresist Metal Contact Pattern	To expose electrical contact areas
18.	Base Width Adjustment Diffusion	Adjust for β = 100 ± 20

4.1.2 Dielectric Isolation Bipolar Transistors

Figure 4-2 shows a dielectrically isolated bipolar transistor in cross section and Figure 4-3 illustrates the dielectric isolation fabrication steps.

The dielectric isolation technique used to fabricate the MCD3 substrates has the following processing sequence:

1.	Starting Material	0.6 ± 15Ωcm N-type <100> 8 mils thick silicon
2.	Initial Oxidation	6-1/2 fringes SiO_2 (sodium light; ≈ 13,000 Å thick)
3.	Photoresist Isolation	To provide dielectrically isolated areas
4.	Silicon Etch	Etch (2-HF; 15-HNO_3; 5-CH_3COOH) to 25μ depth
5.	Buried Layer N+ Diffusion	Sb, monitor wafer 3Ω cm N-type, sheet resistance 18Ω/□, depth 3.5μ

6.	Dielectric Oxide	16,000 Å
7.	Poly Epitaxial Deposition	Deposit ≈ 6 mils, < 0.01Ωcm N-type, polycrystalline silicon
8.	Parallel Lap	Lap ≈ 1 mil off poly deposit to insure a flat and bump-free surface. Forms mounting surface for Step 9
9.	Isolation Jig Lap and Mechanical Polish	Lap off original substrate to expose islands of single crystal silicon. Final polish 0.1μ alumina
10.	Base Mask Oxide	11,000 Å
11.	Photoresist Base	To expose base areas
12.	Base Deposition	B_2O_3, sheet resistance 180Ω/□, depth 2.5μ
13.	Emitter Mask Oxide	11,000 Å
14.	Photoresist Emitter	To expose emitter areas
15.	Emitter Deposition	P_2O_5, sheet resistance 3.5Ω/□, depth 2.5μ
16.	Final Oxide	16,000 Å
17.	Metal Contact Photoresist	To expose device electrical contact areas
18.	Base Width Adjustment Diffusion	Adjust for beta = 100

Table 4-II compares dielectrically isolated and buried layer epitaxial integrated circuits.

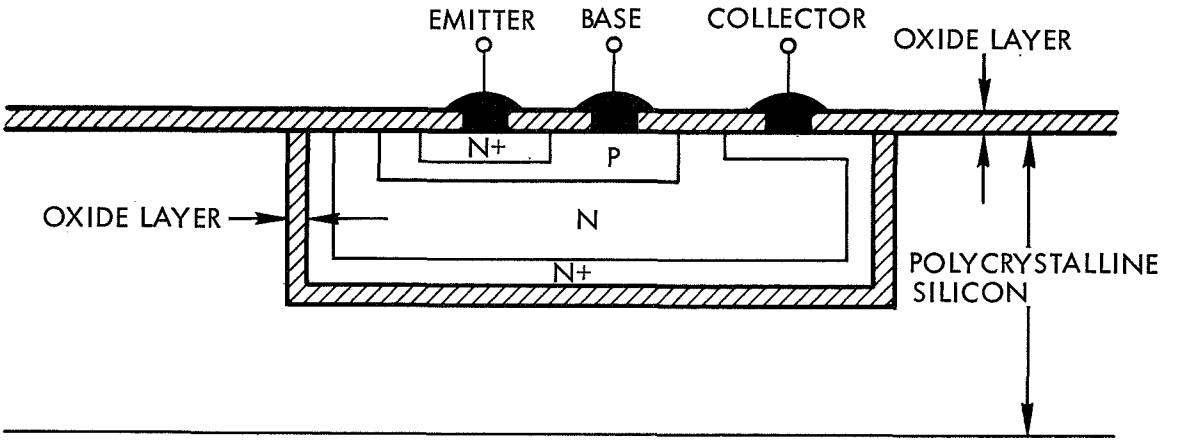


Figure 4-2. Cross Section of Dielectrically Isolated Transistor

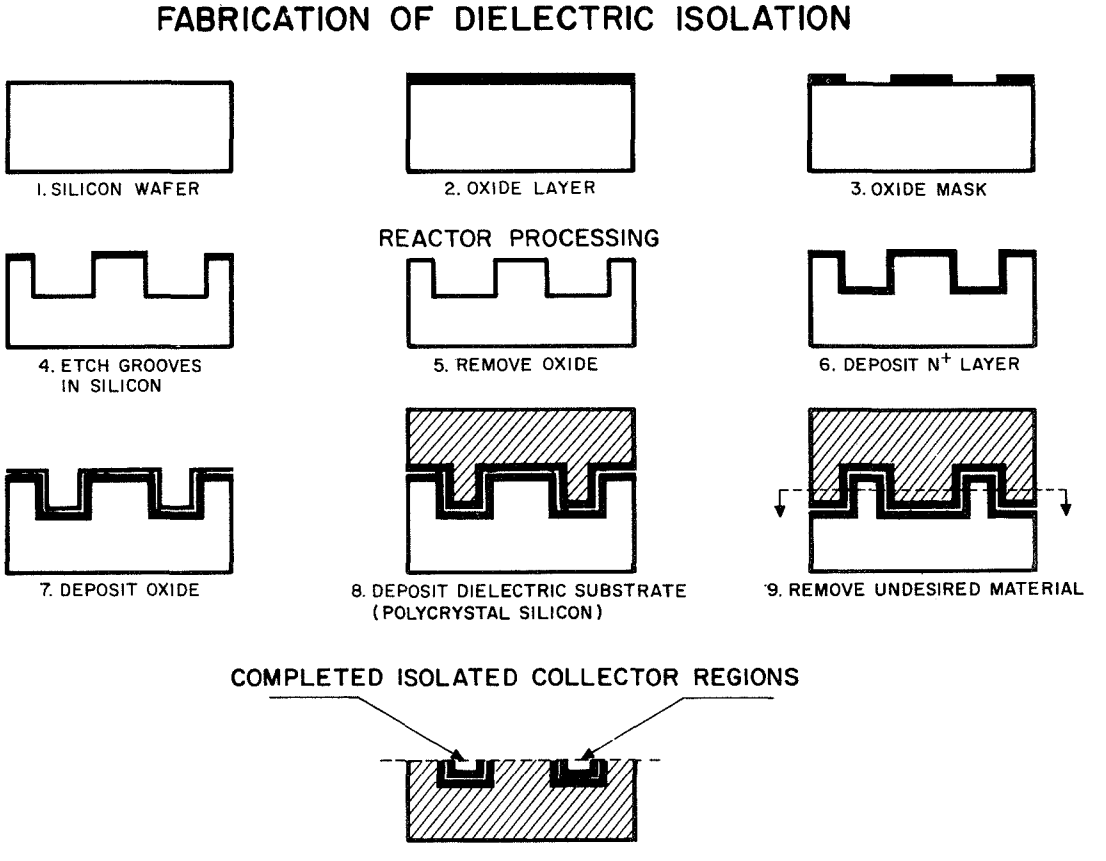


Figure 4-3. Dielectric Isolation Fabrication Steps

TABLE 4-II. COMPARISON OF DIELECTRIC ISOLATION WITH CONVENTIONAL CONSTRUCTION

Item	Dielectric Isolation	Buried-Layer Epitaxial
Number of Processing Steps	Few	Many
Potential Yield	High	Moderate
Quality of Semiconductor Active Body	Same as starting wafer	Subject to Epitaxial process variation
Worst Case Impurity	Short, low-temp., shallow junctions	Long, high temp., deep junctions
Thermal Properties	Moderate	Good
Isolation:		
Breakdown Voltage	Unlimited	Limited
Capacitance	Low	High
Space-Charge Field	Low	High
Leakage Current	Low	Moderate
Parasitic Transistor Action with Substrate	Nonexistent	Design problem
Transistor Performance (General)	As good as discrete transistor	Not as good
Transistor Collector Series Resistance	Low	Moderate
General Integral Circuit Compatibility	Good	Good

4.1.3 MOS Capacitors

Figure 4-4 shows a dielectrically isolated MOS capacitor structure in cross section. Note that the oxide layer over the N+ region is thin (1200 Å) compared with the passivation layer (13,000 Å).

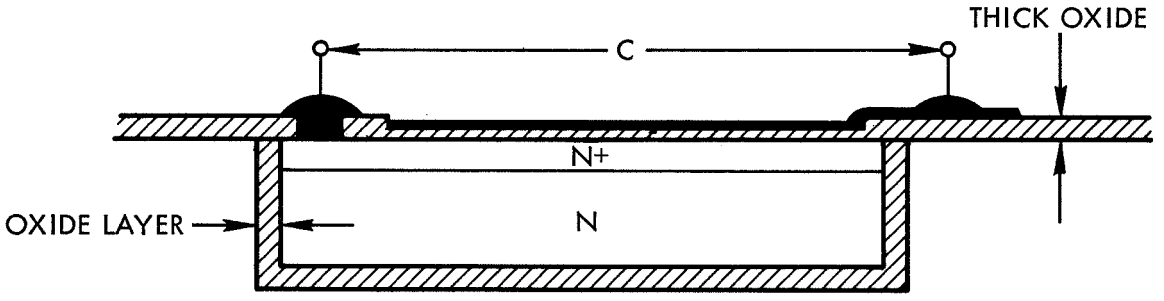


Figure 4-4. A Cross Section of an MOS Capacitor Structure

The structure is fabricated with the following processing sequence.

1.	Starting Material	0.6 ± 15 ohm-cm N-type <100> 8 mils thick silicon
2.	Initial Oxidation	6-1/2 fringes SiO_2, ≈ 13,000 Å thick
3.	Photoresist Isolation	To provide dielectrically isolated areas
4.	Silicon Etch	Etch (2-HF; 15-HNO_3; 5-CH_3COOH) to 25 microns depth
5.	Buried Layer N+ Diffusion	Antimony, monitor wafer 3 ohm-cm N-type, sheet resistance 18 ohms/sq., depth 3.5 microns
6.	Dielectric Oxide	16,000 Å
7.	Poly Epitaxial Deposition	Deposit ≈ 6 mils, <0.01 ohm-cm N-type, polycrystalline silicon

8.	Parallel Lap	Lap ≈ 1 mil off poly deposit to insure a flat a bump-free surface. Forms mounting surface for Step 9.
9.	Isolation Jig Lap and Mechanical Polish	Lap off original substrate to expose islands of single crystal. Final polish 0.1 micron alumina.
10.	N+ Mask Oxide	11,000 Å
11.	Photoresist	To expose N+ area
12.	N+ Deposition	N-type, 2.5 ohm/square
13.	Photoresist Capacitor and Contacts	Defines capacitor and contact area
14.	Grow SiO_2 Dielectric	1200 Å of SiO_2
15.	Photoresist Contacts	To expose silicon for counter electrode contact.
16.	Deposit Metallization	500 Å titanium and 6000 Å of aluminum
17.	Photoresist Metal	Defines electrodes
18.	Metal Sinter	Forms ohmic contact to N+ silicon for counter electrode

4.1.4 Resistors

Figure 4-5 shows a thin film evaporated cermet resistor with metallization in cross section. A buried layer epitaxial substrate is assumed. Note the cermet resistor is also used with the MCD3 dielectrically isolated substrate.

The processing sequence which follows includes all of the surface processing used on a monolithic compatible integrated circuit.

The resistors are fabricated as follows: cermet (Cr:SiO) is evaporated over the wafer giving a sheet resistivity of 300 ohms per square. Photoresist is applied and developed to mask the desired resistor areas. The excess cermet (Cr:SiO) is etched away, leaving resistors. These resistors are then connected into the circuit by the metallization step.

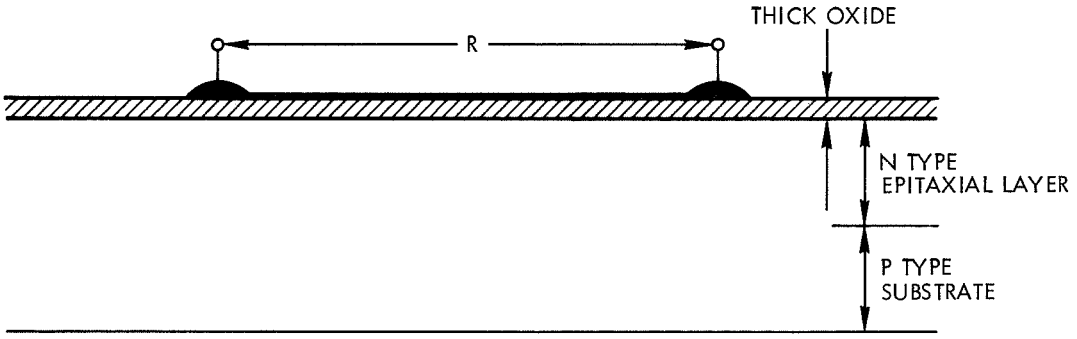


Figure 4-5. Cross Section of Cermet Resistor

After the substrate (epitaxial or isolated) has been processed and the circuit contact holes etched,

1. Metallizing I	Vacuum deposit 600 Å of titanium and aluminum of 0.02 ohms/square sheet resistance
2. Metallization I Sinter	Heat treatment to insure low resistance ohmic contact to silicon
3. Metallization I Etch	
4. Cermet Deposition	Cr:SiO sheet resistance 300 ± 10 ohm/square, thickness ≈ 300 Å
5. Photoresist Cermet	To leave desired cermet for resistors
6. Metallizing II	Identical to Metallizing I, except for aluminum deposition sheet resistance of 0.04 ± 0.01 ohm/square
7. Photoresist Metallizing II	To leave desired metal for interconnections
8. Metallizing II Sinter	Heat treatment to insure low resistance ohmic contact to cermet
9. Wafer Electrical Function Test	

4.2 DEVICES

The following is a brief description of the integrated devices used in the TRW modules.

4.2.1 MCD1

Figure 4-6 shows the MCD1 assembly drawing. This substrate is fabricated with the buried layer epitaxial technique. The clear area around the transistor cluster is available for resistors, interconnections, and bonding pads. Crossunders are provided specifically in four locations and generally in any of the transistor positions. A transistor structure can be used as a transistor, diode, capacitor, or crossunder, as determined by the placement of the contact holes in the oxide, aluminum interconnection, and application of the circuit. The CS01A and VR03 circuits use this substrate.

Figure 4-7 shows the transistor lateral geometry in detail. Note that the smallest mask spacing is 0.25 mil.

4.2.2 MCD3

Figure 4-8 shows the MCD3 assembly drawing. This substrate is fabricated with dielectric isolation to eliminate the dc substrate parasitics associated with the PNP transistors. The VR34 and VR35 voltage regulator circuits use this substrate.

Five types of transistors are included in the MCD3. These are:

a) Low Current NPN. Shown in Figure 4-9. This transistor is used in all NPN positions except for the regulating element in the positive supply line and the switch in the negative supply line. Nominal h_{FE} of 100 at I_c = 5 mA is typical. This device is also used as forward biased diodes and reverse biased emitter-base diodes (voltage reference).

b) High Current NPN. Shown in Figure 4-10. This transistor is used as the regulating element in the positive supply line and the switch in the negative supply line. Nominal h_{FE} of 100 at I_c = 60 mA is typical. Collector parasitic bulk resistance, r'_c, is typically less than 15 ohms.

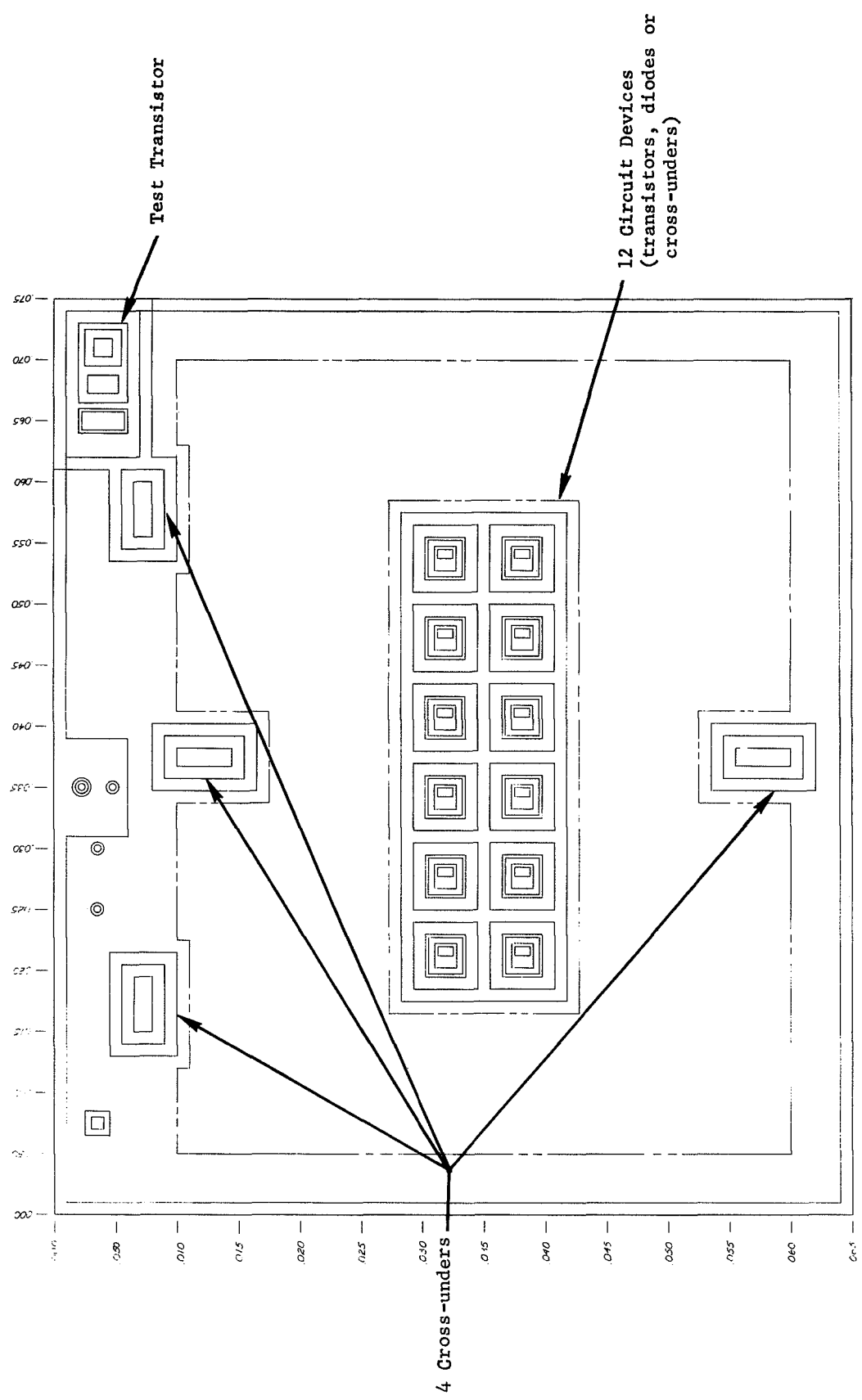
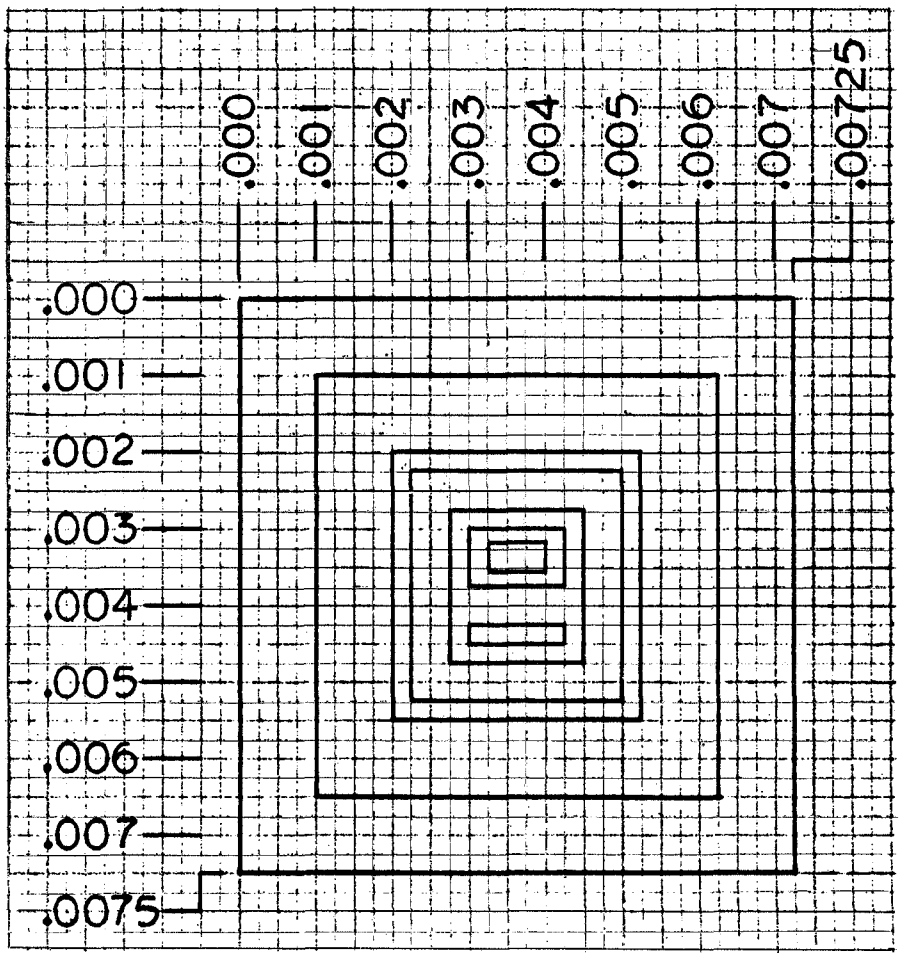


Figure 4-6. Multi-Circuit Die (MCD1) Assembly Drawing



Scale 400:1

Figure 4-7. Multi-Circuit Die (MCD1) Transistor Lateral Geometry

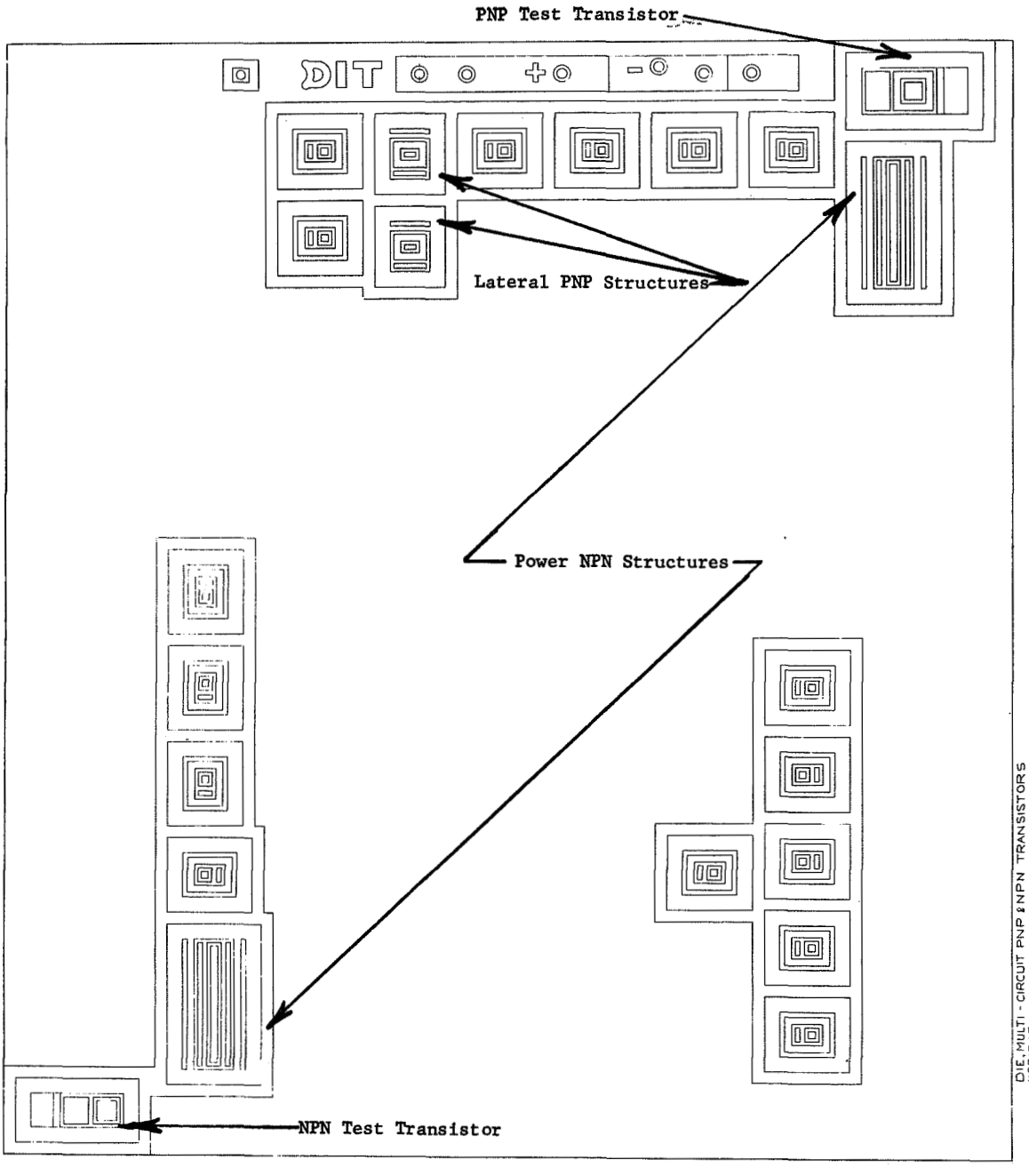
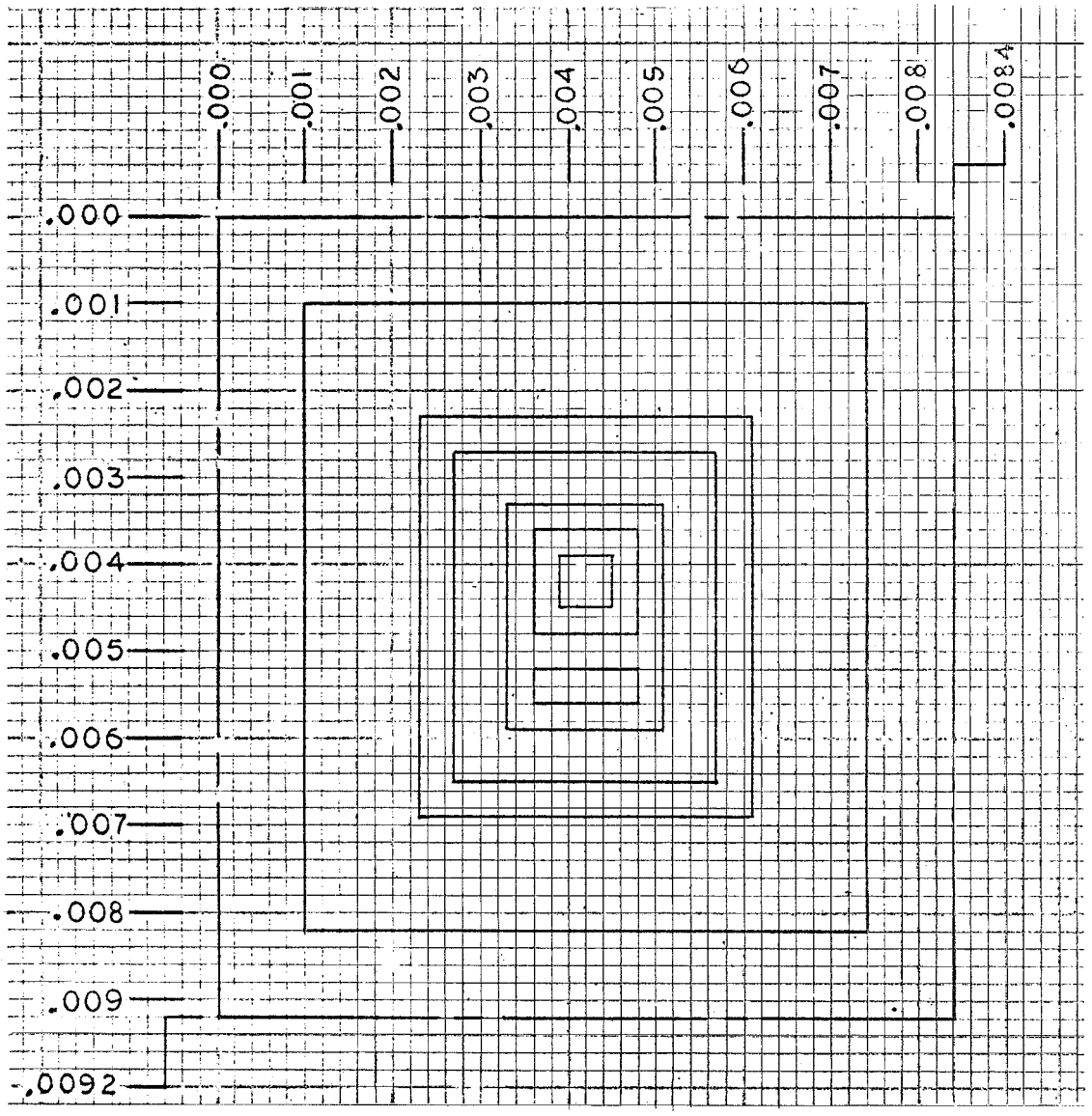


Figure 4-8. Multi-Circuit Die (MCD3)
Assembly Drawing



Scale 500:1

Figure 4-9. NPN Low Current (MCD3) Transistor Lateral Geometry

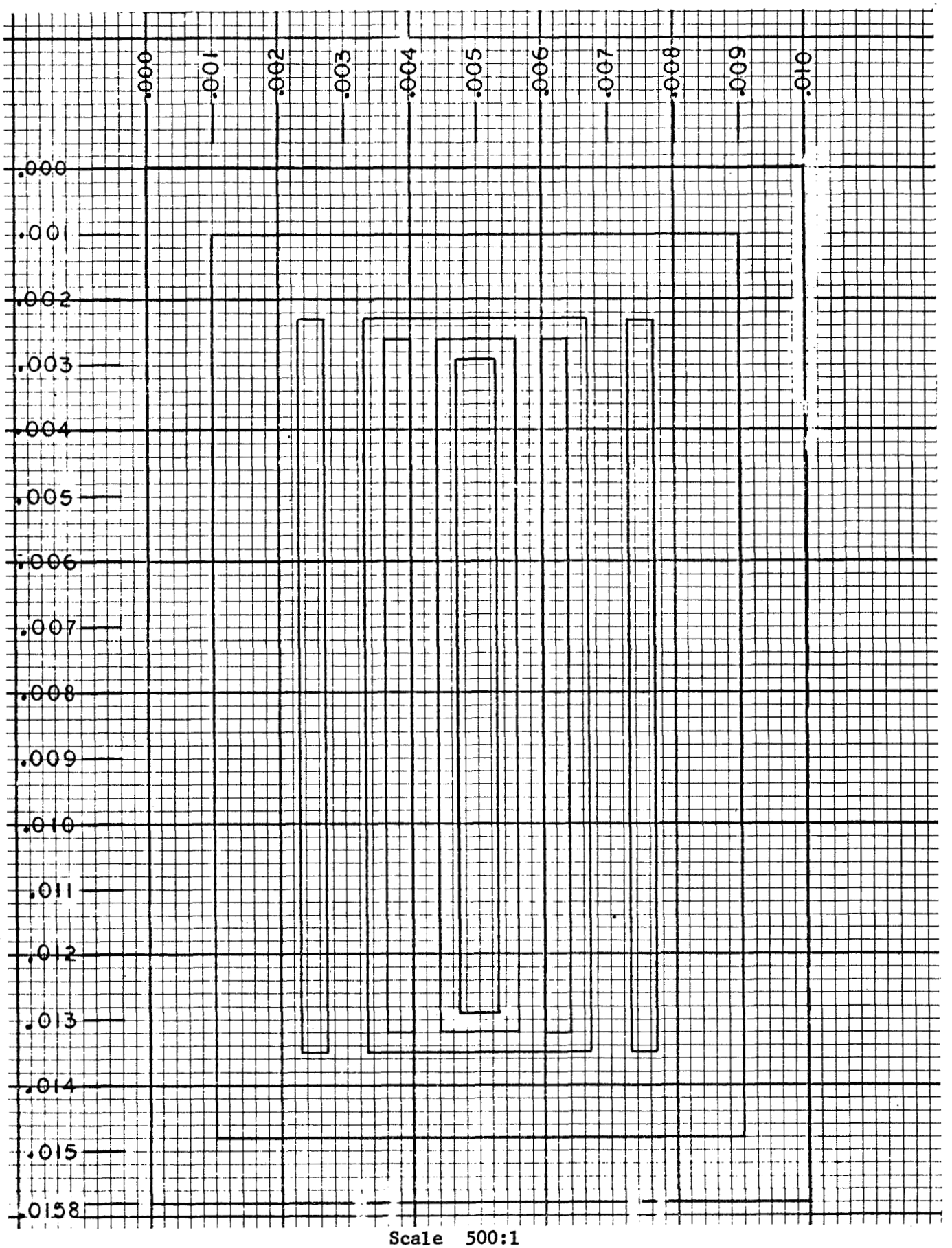


Figure 4-10. NPN High Current (MCD3) Transistor Lateral Geometry

c) Lateral Geometry PNP. Shown in Figure 4-11. This transistor is used (in a composite configuration) as a constant current generator and as a current monitor for short circuit protection. Nominal h_{FE} of 2 at I_c = 100 μA is typical.

d) NPN Test Transistor. Shown in Figure 4-12. This transistor is used primarily for device check before metallization.

e) PNP Test Transistor. Shown in Figure 4-13. This transistor is used primarily for device check before metallization.

Figure 4-14 shows a special metal transistor test pattern used with the MCD3 substrate.

4.2.3 MCD4

Figure 4-15 shows the MCD4 substrate used in the SCA41 and SCA42. This substrate is fabricated with buried layer epitaxy.

4.2.4 CA01

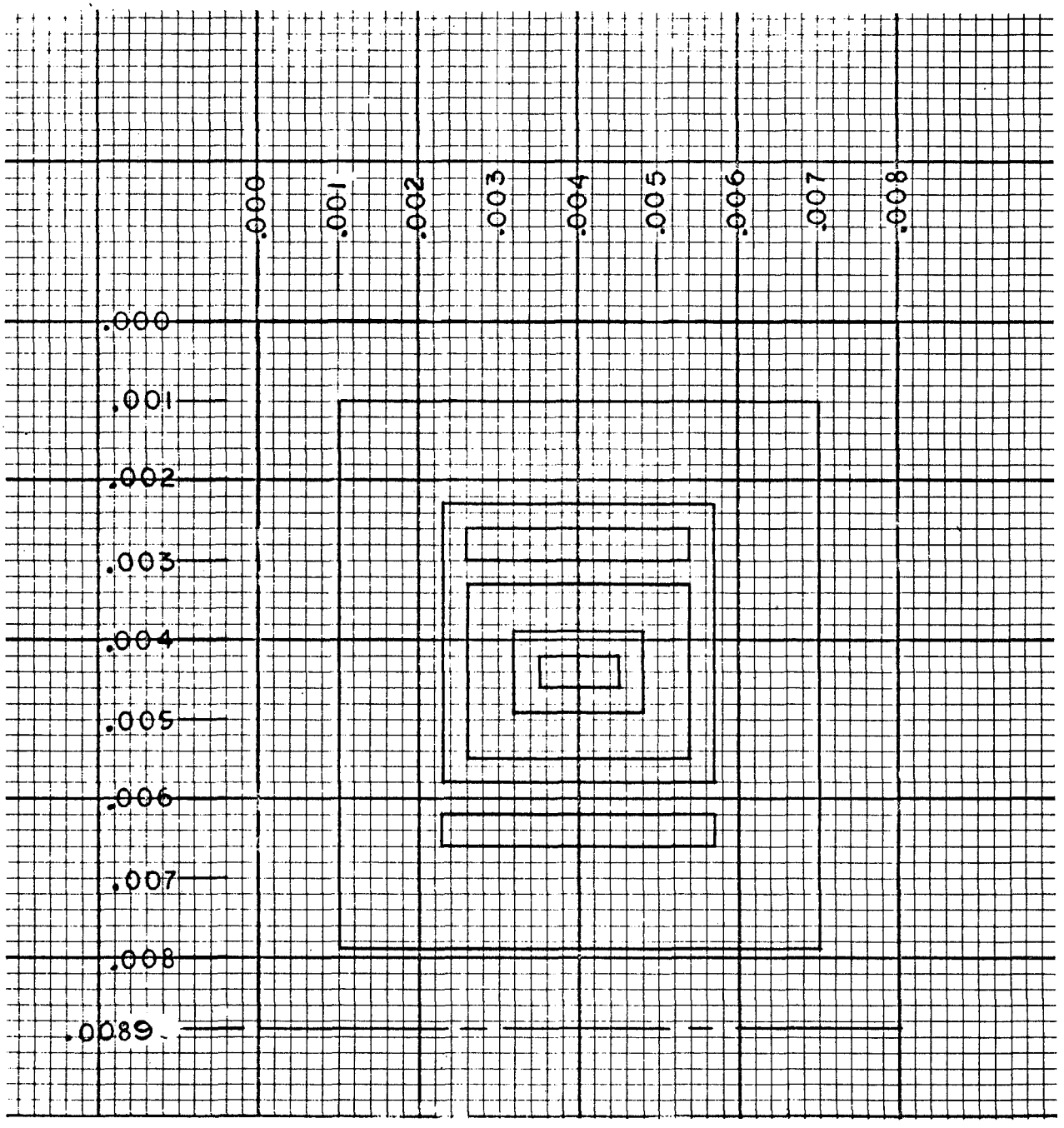
The CA01 is shown in Figure 4-16. Eight separate capacitors are available. The six large sections are approximately 50 pF each. The two small sections are 14 pF each. Fuses in the metal interconnect can be blown out to lower the capacitance values. Each of the eight capacitors has subsections weighted in a binary ratio of 8:4:2:1. See Section 4.2.5 about the description of the fuse-adjustment technique.

4.2.5 Resistors

Resistors 1 K ohms or larger are $\geq$ 0.6 mil wide and exhibit the following characteristics:

Absolute Tolerance	± 20%
Relative Tolerance (on wafer)	± 10%
Ratio Tolerance (adjacent resistors)	± 1%
Ratio Tolerance (nonadjacent resistors)	± 2.5%
Maximum Absolute Temperature Coefficient	200 ppm/°C
Maximum Tracking Temperature Coefficient	10 ppm/°C

Figure 4-17 shows the geometry of a typical resistor adjustment fuse link. Probes are placed on the metal interconnect and current is passed



Scale 500:1

Figure 4-11. PNP (MCD3) Lateral Geometry

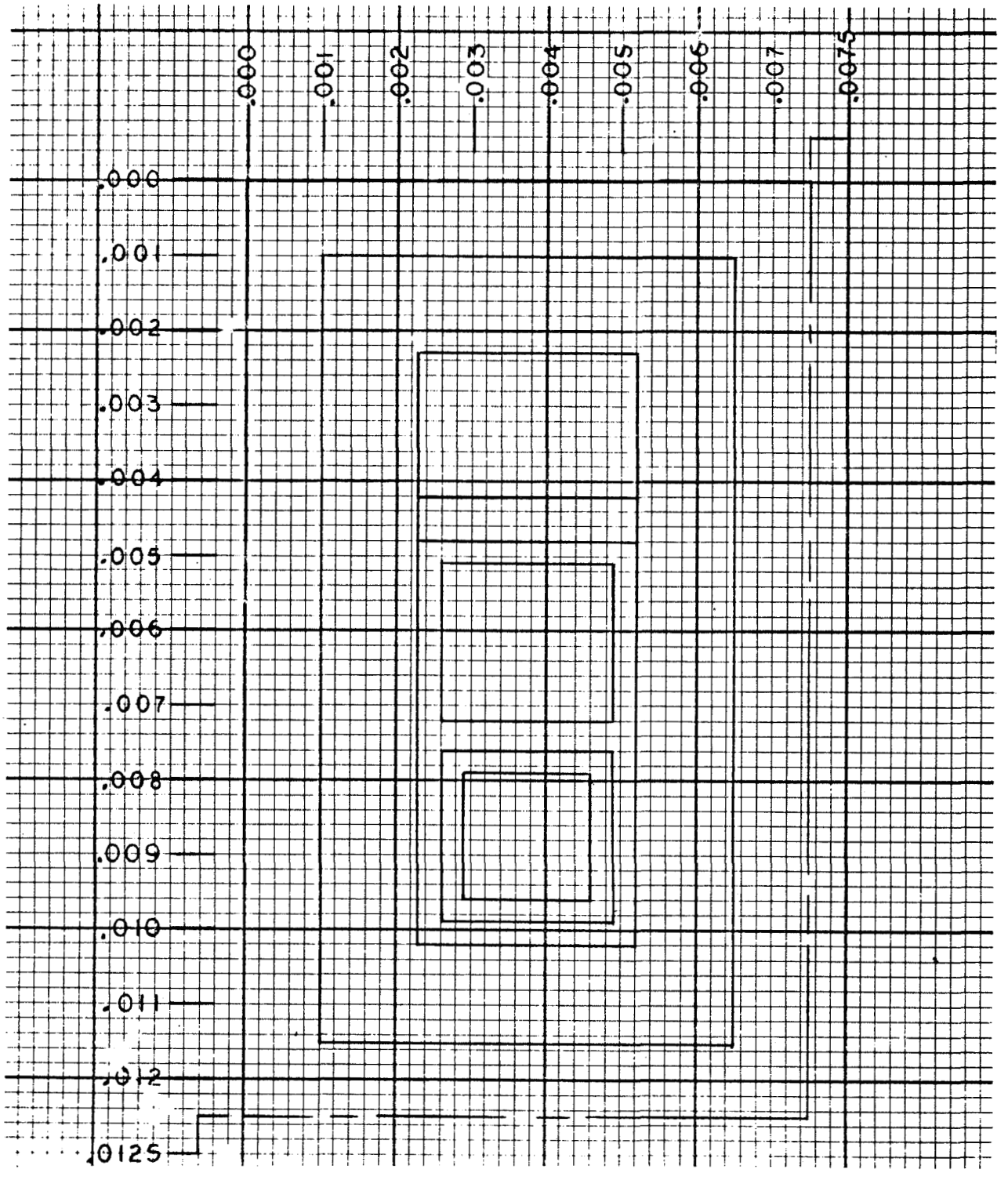


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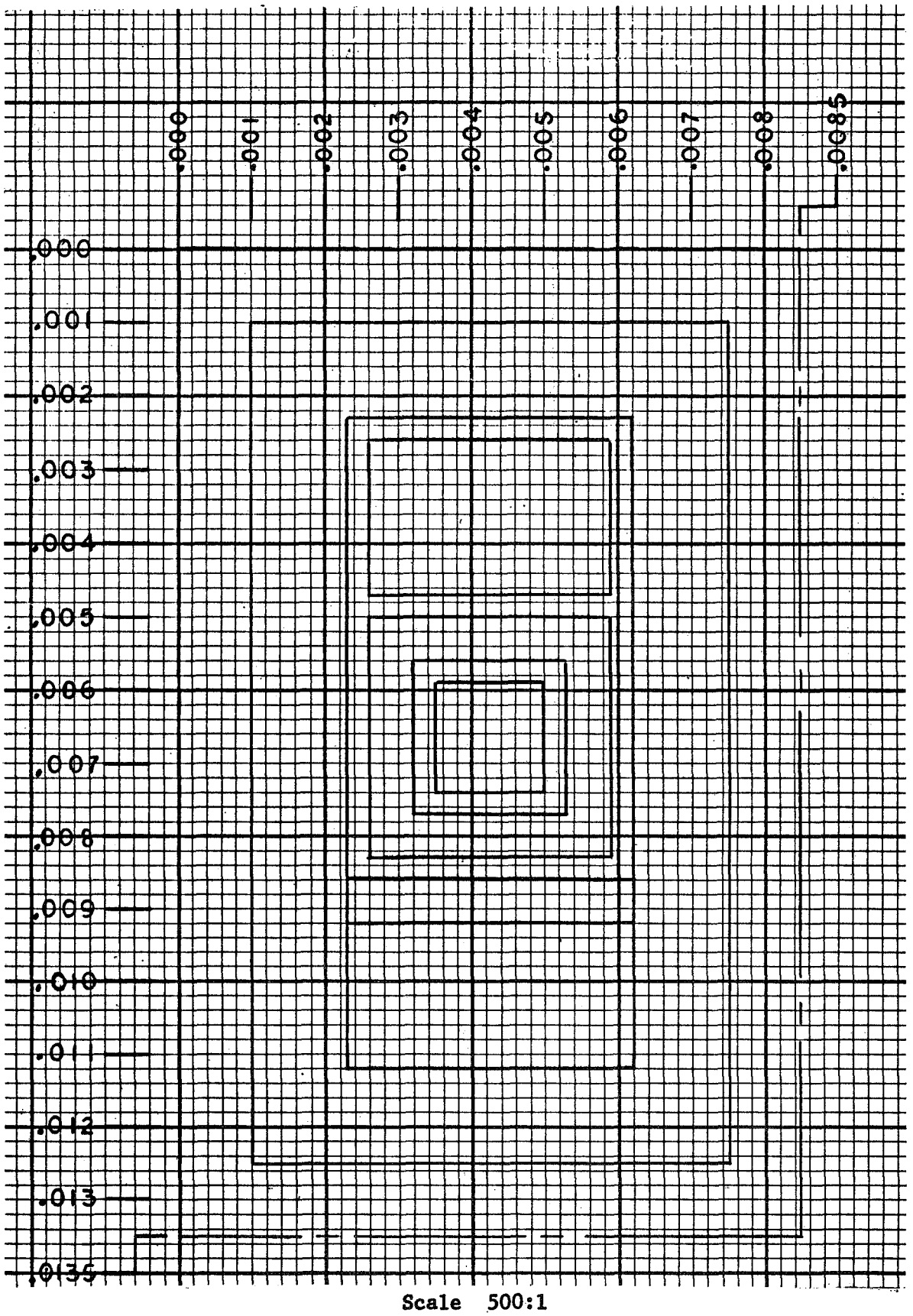
Figure 4-12. NPN (MCD3) Test Transistor



Scale 500:1

Figure 4-13. PNP (MCD3) Test Transistor

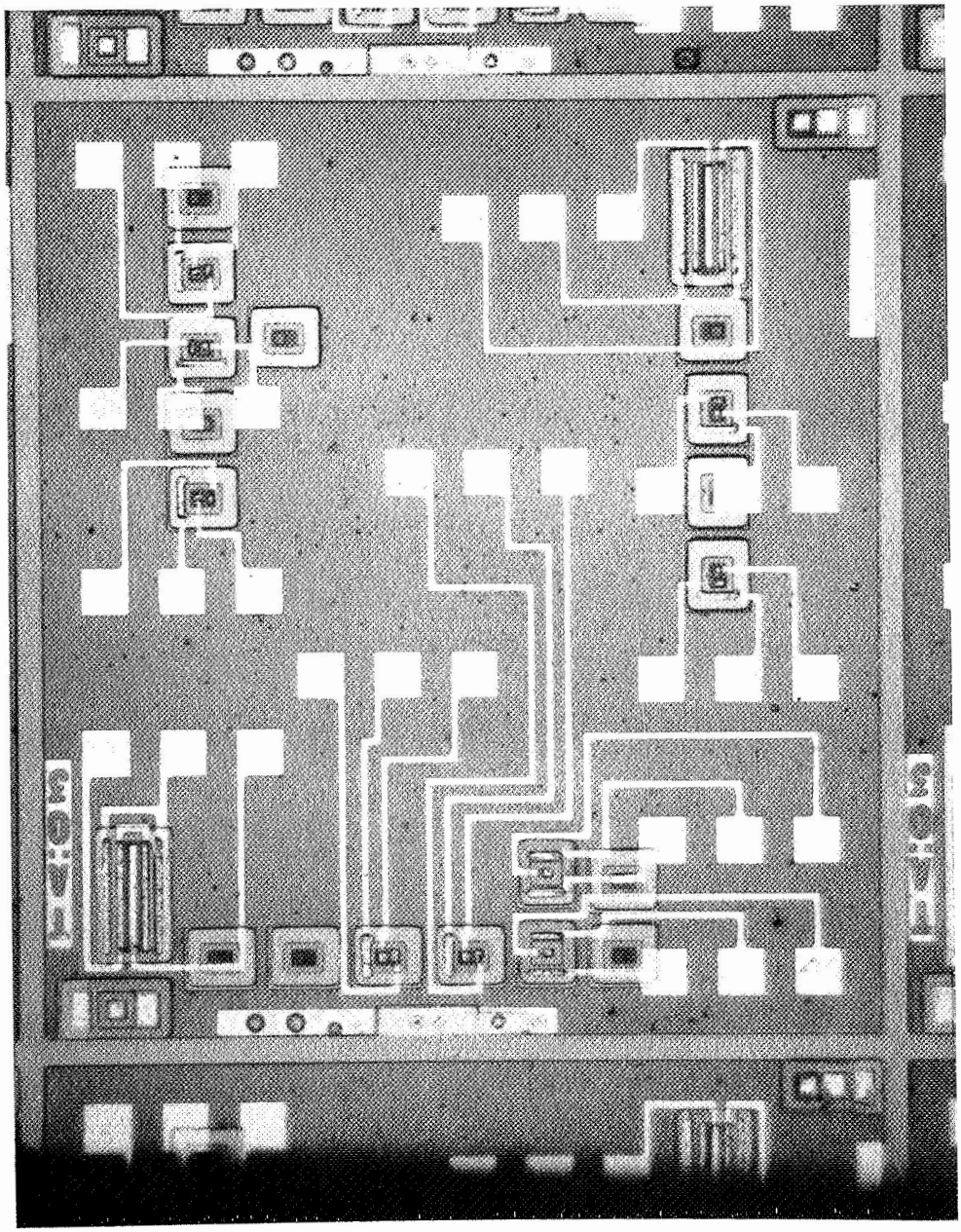


Figure 4-14. Photograph of MCD3 with TA03 Test Pattern

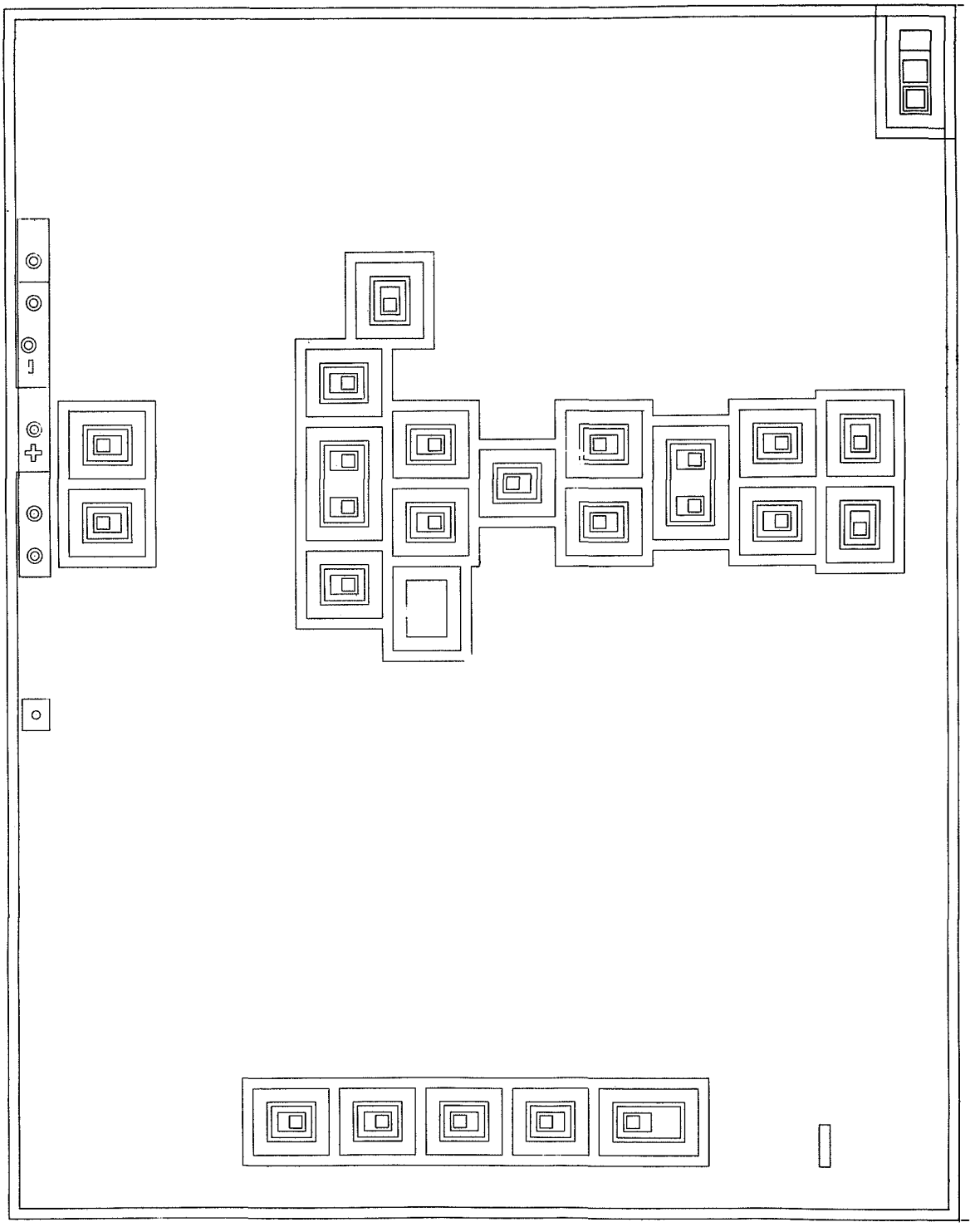


Figure 4-15. MCD4 Substrate

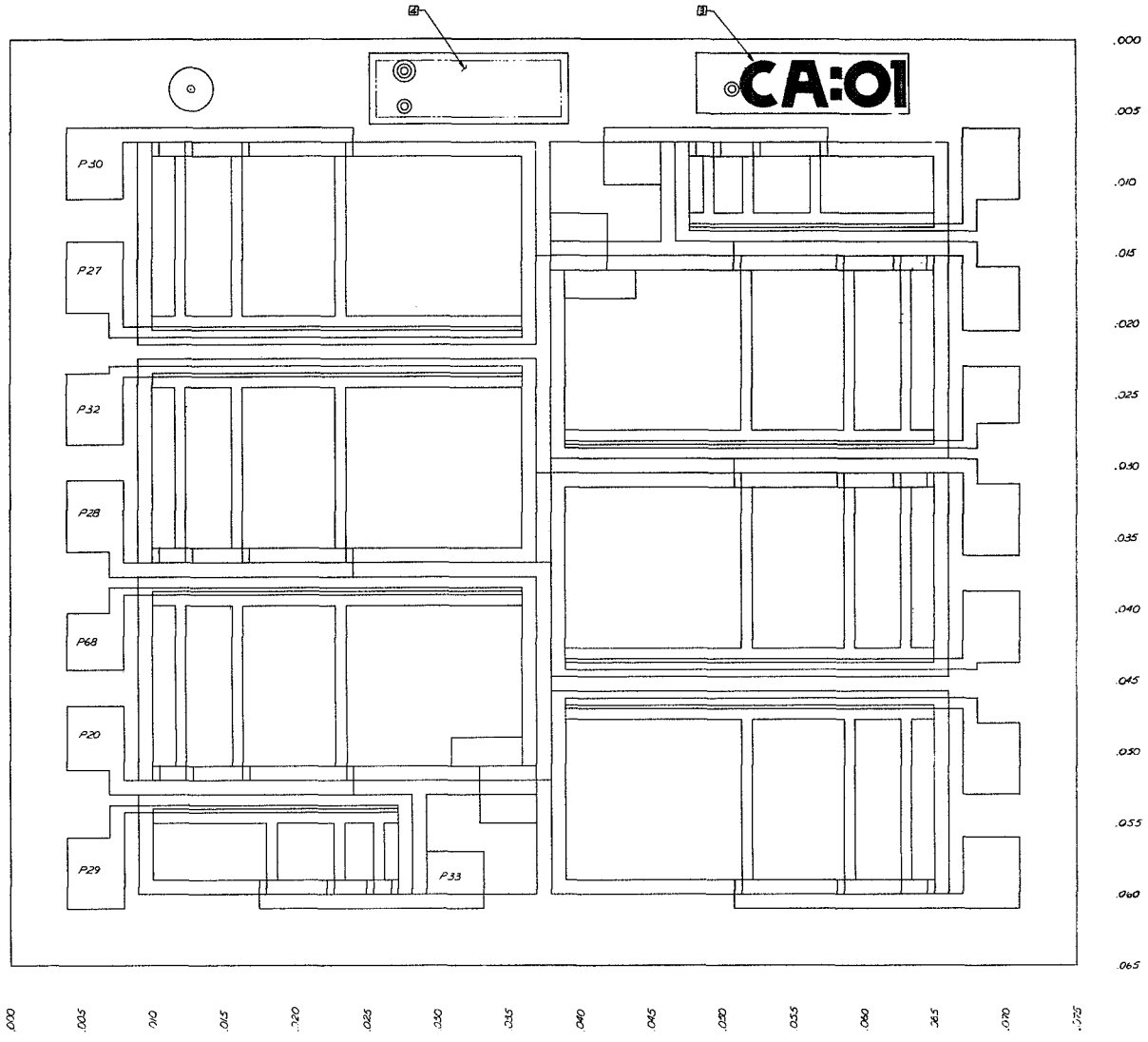


Figure 4-16. CA01 Lateral Geometry

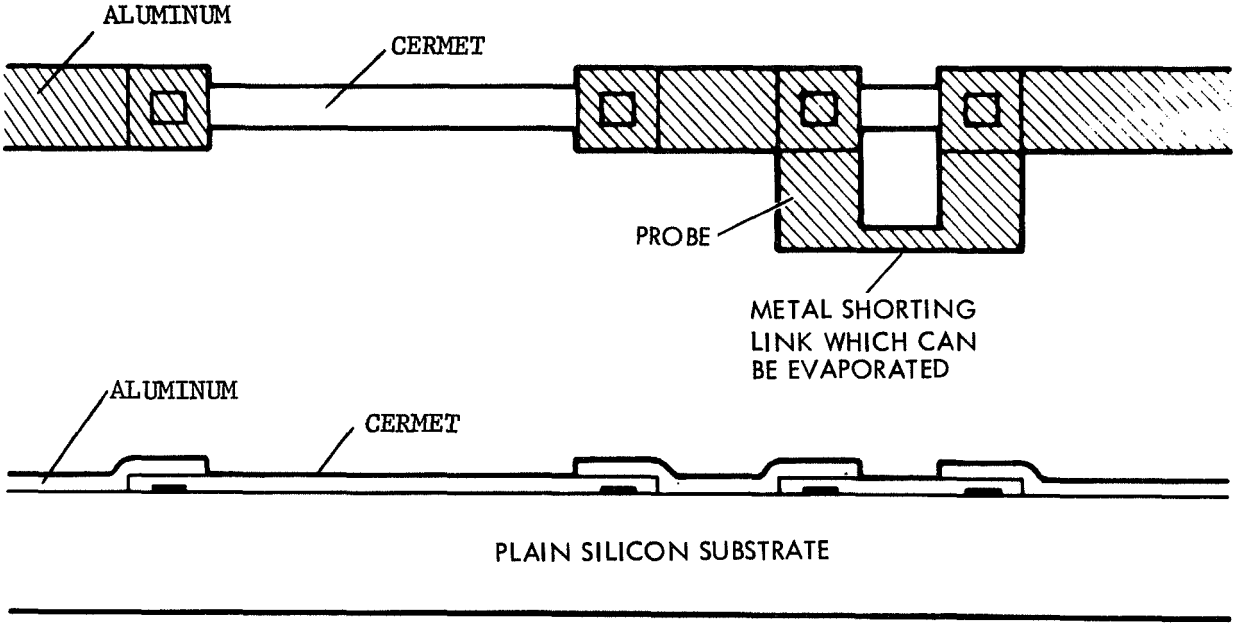


Figure 4-17. Typical Geometry of Adjustable Feedback Resistor

through the metal. It melts and opens the shorting link. Figure 4-18 is a photograph of a fuse link before and after probing. Note how the aluminum melts and leaves a clean break in the interconnection pattern.

4.3 PACKAGING

Only the packaging of the TRW integrated circuit modules is considered in this section.

4.3.1 Packages

The following drawings specify the three types of packages used.

Figure 4-19: (1/4" x 3/8") flat pack - Used for the VR34, VR35, SCA41, SCA42, and CA01

Figure 4-20: (3/8" x 3/8") flat pack - Used in the power converter

4.3.2 Die Attachment - Wire Bonding - Package Sealing

Two types of die attachment techniques were incorporated:

a) Thermal Bond - Using an AuSi alloy as the bonding agent (GTR, GMR, MM1, LSG05)

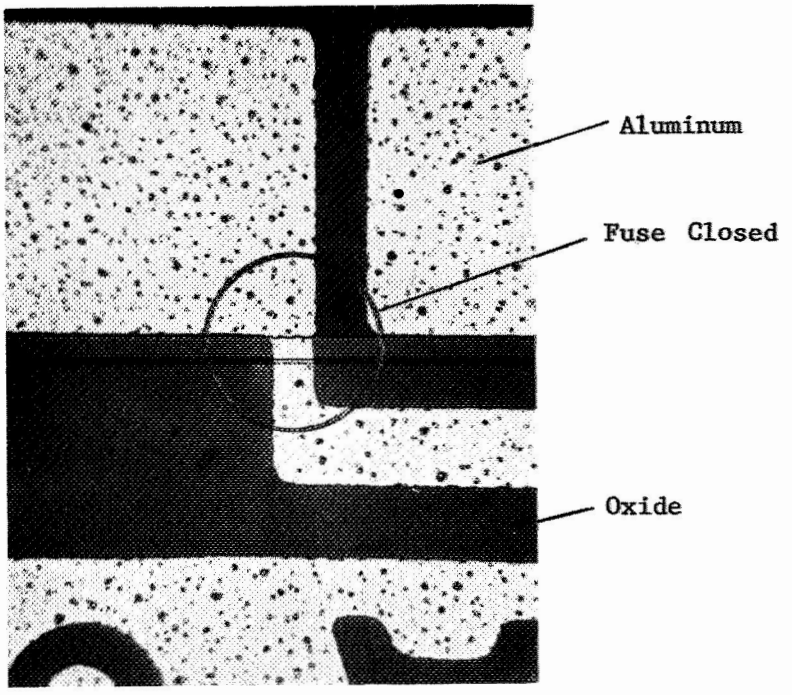
b) Conductive Epoxy Cermet - Using DuPont Silver preparation, Electronic Grade 5504-A, A high temperature epoxy (power converter flat pack)

The thermal bond is the preferred technique for establishing a reliable die attachment. The conductive epoxy is used only in applications in which the die must potentially be extracted and replaced in multi-die packages.

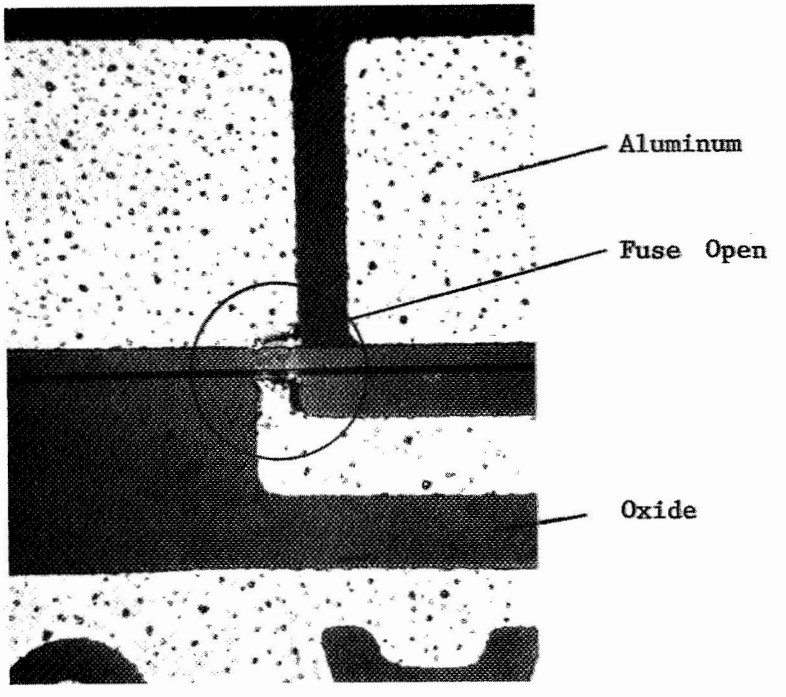
Thermal compression ballbonding with 1.5 mil gold wire is used for wire attachment. Sealing is accomplished using a gold alloy solder in an inert atmosphere.

4.4 NEW TECHNOLOGY

This contract did not require the development of any new technology.

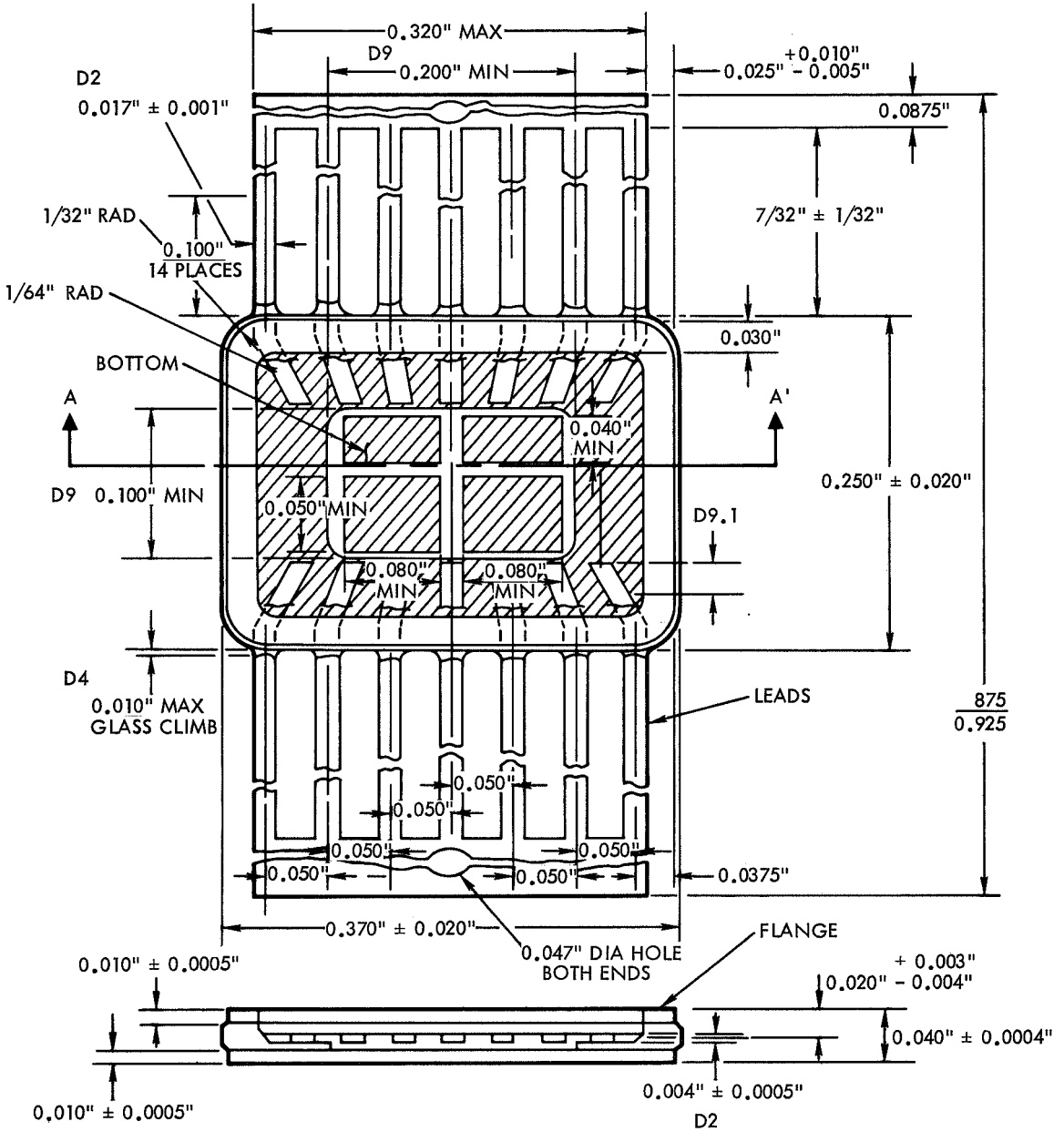


Before



After

Figure 4-18. Photograph of Fuse Link Operation



SECTION A A

Figure 4-19. 1/4" x 3/8" Flat Pack Drawing

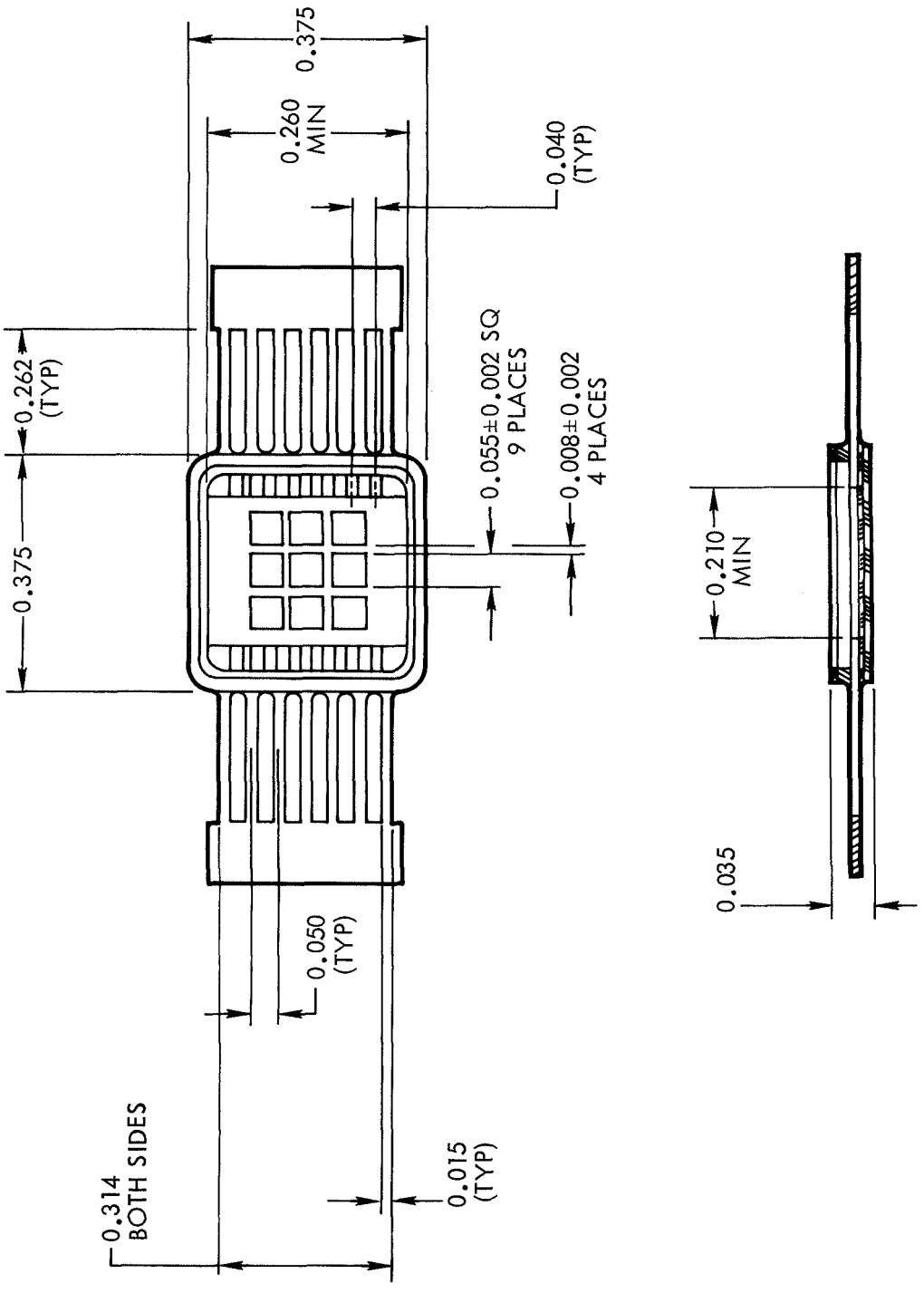


Figure 4-20. 3/8" x 3/8" Flat Pack Drawing for Power Converter

5. TESTING

5.1 GENERAL

The purpose of this test procedure is to outline a sequence of functional tests to verify compliance with the contract specifications. The tests and results demonstrate the performance of the Signal Conditioner modules.

A multipurpose printed circuit board is used to interconnect the micro-electronic modules. Figures 5-1 and 5-2 show typical amplifier and power source cards, respectively. Table 5-I shows the board pin connections. Ten amplifier cards and five power source cards comprise the contract hardware delivery items.

Refer to Appendix A for the performance specification test criteria

5.2 TEST DESCRIPTION

Tests 1, 2, and 6 are performed at five temperatures: $-35^{o}C/-30^{o}F$, $-18^{o}C/0^{o}F$, $+25^{o}C/+75^{o}F$, $+71^{o}C/+160F$, $+95^{o}C/+200^{o}F$. The eight functional steps are:

Function #1

The amplifier dc output voltage offset and output noise is measured with the test connection shown in Figure 5-3. The amplifier input is internally biased to ground, so the source configuration is a floating 360-ohm resistance, as specified. The amplifier output is connected to a dc digital voltmeter and an oscilloscope with a 15 MHz pass band.

The amplifier is temperature cycled from $-35^{o}C$ to $+95^{o}C$. The output voltage is recorded together with the peak-to-peak noise. The oscilloscope simultaneously monitors the amplifier dynamic stability

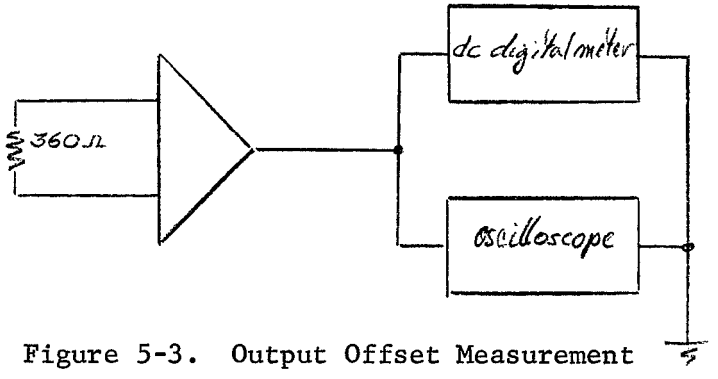


Figure 5-3. Output Offset Measurement

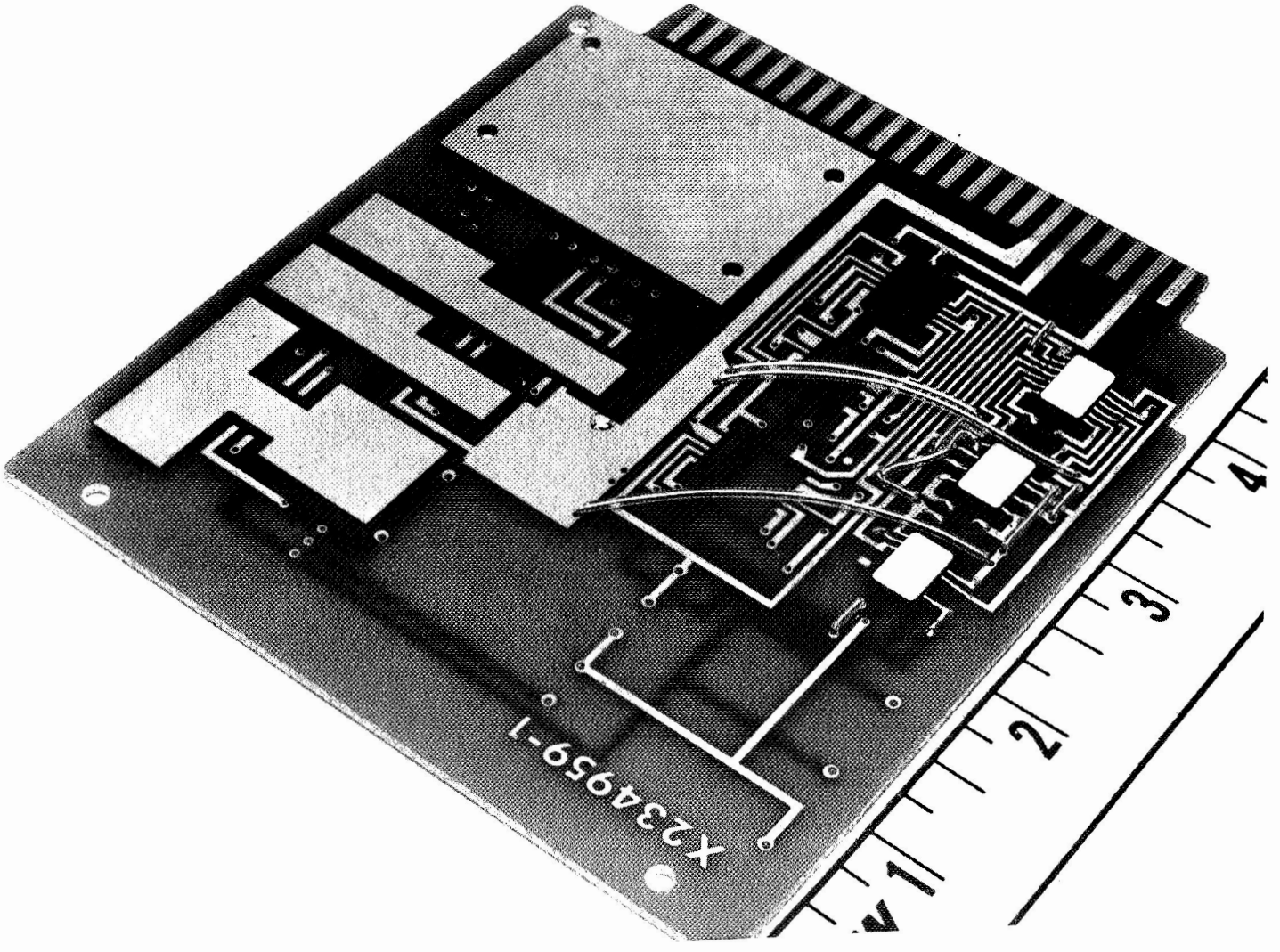


Figure 5-1. Photograph of Amplifier Assembly

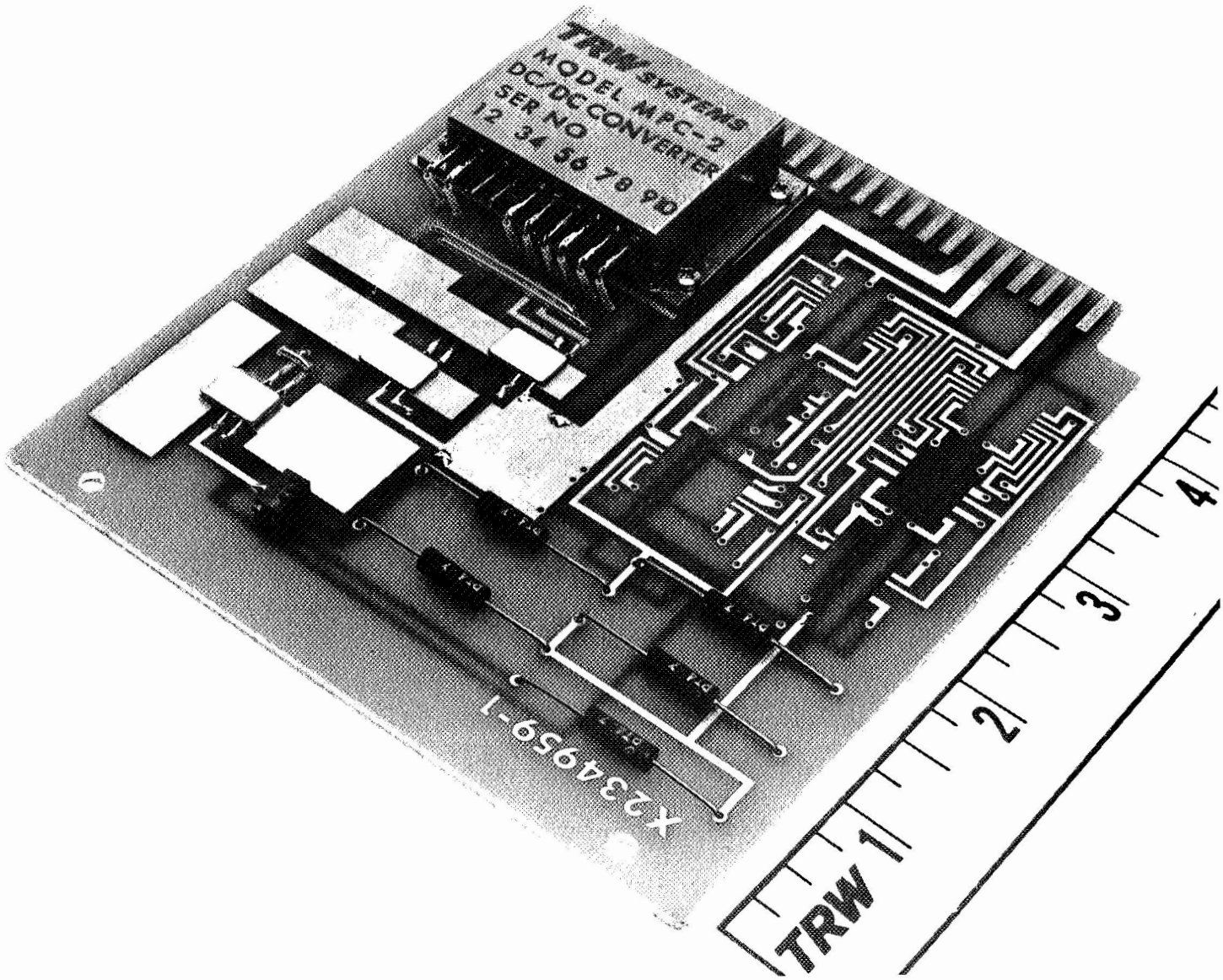


Figure 5-2. Photograph of Power Source Assembly

TABLE 5-I. PRINTED CIRCUIT BOARD PIN CONNECTIONS

Pin Designation	Correction
1	Converter input common (-)
2	Converter input (+28 volt)
3	Converter output (-) } (23 volts)
4	Converter output (+) } (23 volts)
5	Converter output (-) } (23 volts)
6	Converter output (+) } (23 volts)
7	Converter output (+) } (16.5 volts)
8	Converter output (-) } (16.5 volts)
12	VR34 Output (+10 volts)
14	VR35 Output (+15 volts)
15	Ground monitor
16	VR35 Output (-15 volts)
17	Ground
18	Amplifier Output
21	Amplifier Input - B
22	Amplifier Input - A

Function #2

The amplifier dc gain is measured with the test connection shown in Figure 5-4. A precision divider attenuates the input signal allowing the input to be measured at a high level. The low impedance arm of the divider is chosen to insure that the amplifier input impedance does not significantly load the divider.

The dc digital voltmeter monitors either the input or output as determined by the calibrate switch, S_{3A}. Measuring the input voltage to the resistance divider and the output voltage of the amplifier allows the amplifier dc gain to be calculated, assuming the resistance divider is sufficiently accurate. The gain is measured from zero to full scale output. The amplifier output impedance is measured (or shown to be less than the specified value) by loading the amplifier output via S_4 and measuring the resulting change in output voltage.

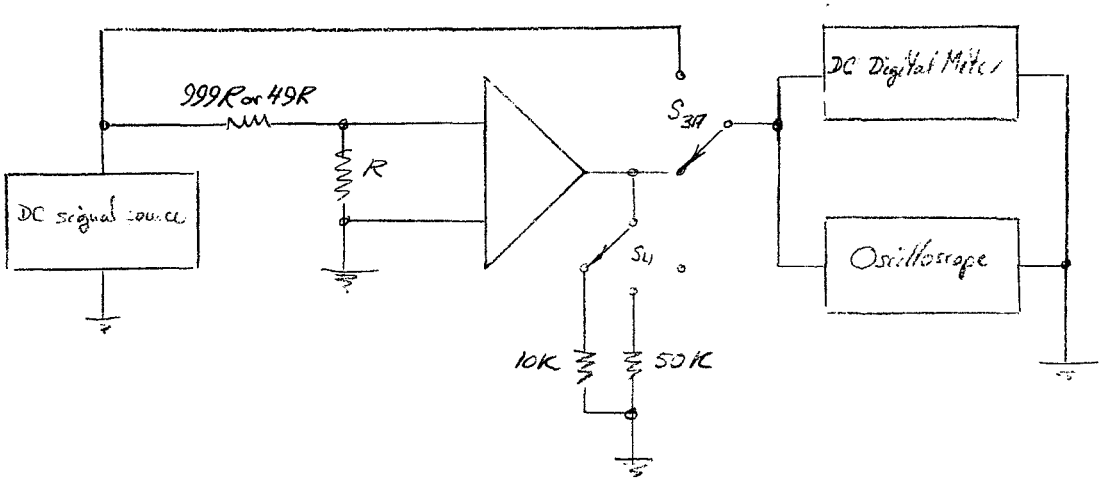


Figure 5-4. DC Gain Output Impedance Measurement

Function #3

The amplifier linearity is measured with the test connection shown in Figure 5-5. The dc source is first set at 0 volts. The DC Digital Meter then indicates the amplifier offset, which is recorded. Next, the DC Signal Source is set to +5.0 volts. The potentiometer is then adjusted so the DC Digital Meter reads the offset value previously recorded. The DC Signal Source is then set for +1, +3, +4, +5 volts, etc. The deviation the DC Digital Meter reads from the original offset is the deviation from linearity.

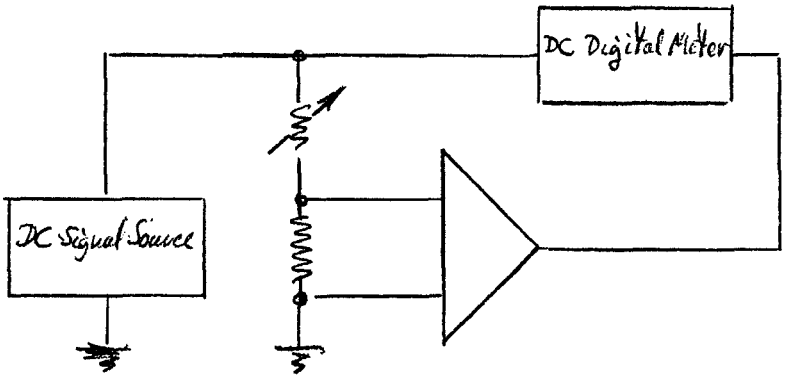


Figure 5-5. Linearity Measurement

Function #4

The amplifier frequency response is measured with the test connection shown in Figure 5-6. A precision divider attenuates the input signal allowing the input to be measured at a high level. The low impedance arm of the divider is chosen to insure that the amplifier input impedance does not significantly load the divider.

The DC Digital Voltmeter monitors either the input or output as determined by the calibrate switch, S_{3A}. Measuring the input voltage to the resistive divider and the output voltage of the amplifier allows the amplifier ac gain to be calculated as a function of frequency, assuming the resistive divider is sufficiently accurate. The output voltage swing is set to $\pm$ 1 volt to insure linear operation in the negative direction. The amplifier output swing limits can be observed on the oscilloscope by increasing the ac input signal until both positive and negative limiting occurs.

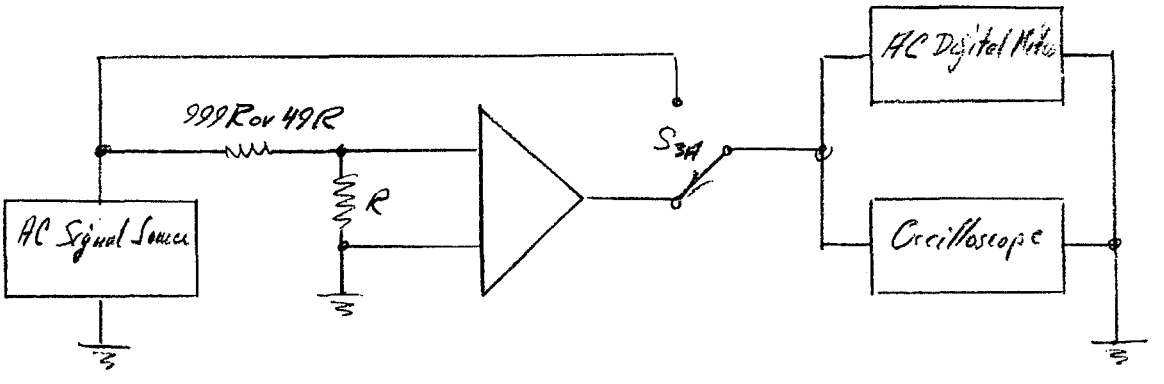


Figure 5-6. Frequency Response Measurement

Function #5

The common-mode rejection is measured with the test connection shown in Figure 5-7. The ac signal source is monitored when the calibrate switch, S_{3B}, is in the up position and is set to a $\pm$ 1 volt amplitude. The S_{3B} switch is then set to monitor the amplifier output and a reading taken. These measurements allow the common-mode gain to be calculated. The common-mode rejection is the ratio of the differential mode gain to the common-mode gain.

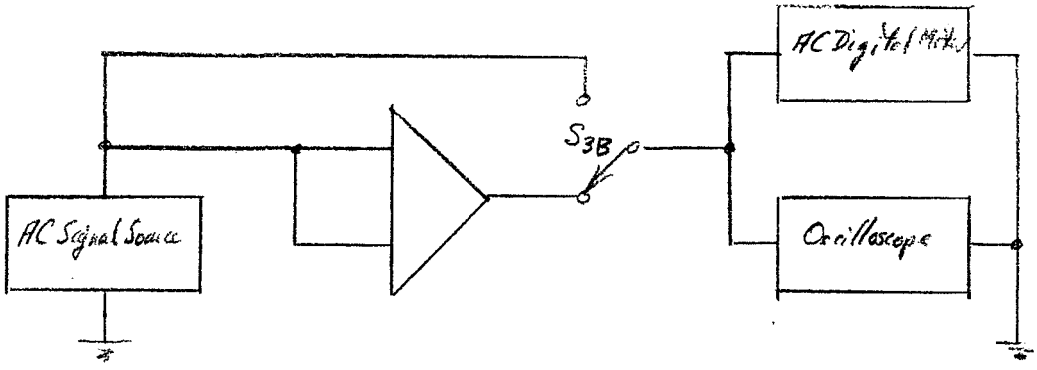


Figure 5-7. Common-Mode Rejection Measurement

Function #6

The input resistance m easurement is made with the connection shown in Figure 5-8. Making the assumption that the amplifier input resistance is dominated by the biasing resistors which are connected from each input transistor base to ground, the input resistance is simply made with an ohmmeter (the amplifier power is OFF). Sides A and B are selected by switch S_5. This assumption is valid since the actual amplifier input resistance is more than five-hundred times the biasing resistor impedance. Note that the specified differential input impedance refers to the sum of R_{in-A} and R_{in-B}.

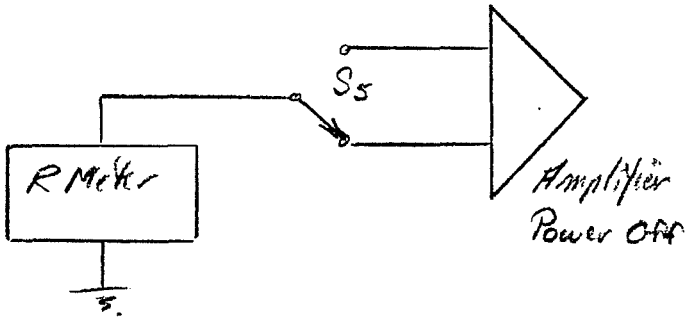


Figure 5-8. Input Impedance Measurement

Functions #7, #8, and #9

Figure 5-9 shows the connection for making measurements of the transducer excitation voltage and amplifier supply voltages. The DC Digital Meter measures the voltages as a function of temperature and input battery voltage. The oscilloscope is used to measure the peak-to-peak noise.

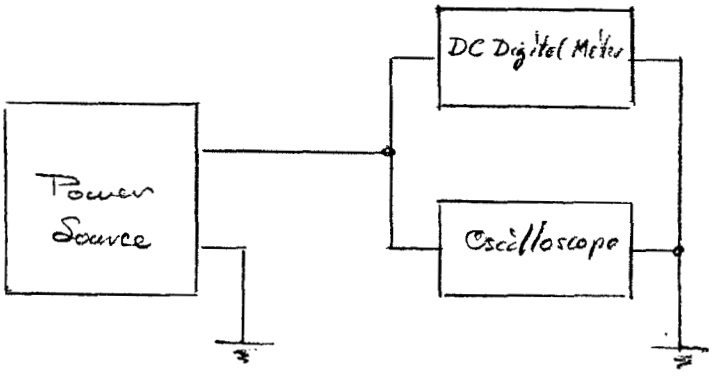


Figure 5-9. Power Source Voltage Measurements

5.3 TEST UNIT DESCRIPTION

Figures 5-10 and 5-11 show the front and back views, respectively, of the Signal Conditioning Amplifier and the Power Source Test Unit. Figure 5-12 shows the test set connections. Figure 5-13 shows the test set wiring.

The following describes the function of the test unit.

5.3.1 Front Panel

1) Power - A power supply is included in the tester to convert 110 volts/60 Hz ac to +28 volts dc nominal. The power switch interrupts the 110 volt/60 Hz ac input. An indicator light is turned on when the test unit is turned on. A switch labeles (22, 32, 28) allows the operator to select the specified tolerances on the +28 volts. This voltage, which is the input to the power source, can be monitored on the terminals marked E_{in} in the Internal Connections section.

2) Controls - A rotary switch labeled "Module Select" selects the power source to be energized and the amplifier to be measured. The rotary switch labeled "Function" selects the measurements to be performed. The toggle switch, R_{in}, selects the A or B side of the amplifier input to measure the input impedance. The "Normal-Calibrate" toggle switch is used to select a measurement of either the input or output of the amplifier in the gain and CMR measurements. The R_L toggle switch selects the resistive load on the amplifier output. The 10 K position is used to check the amplifier output impedance. The 50 K and open circuit positions are specified.

3) Linearity Calibrate - These controls are used to calibrate the linearity measurement for a +5 volt input voltage. Separate controls are provided for the two gains.

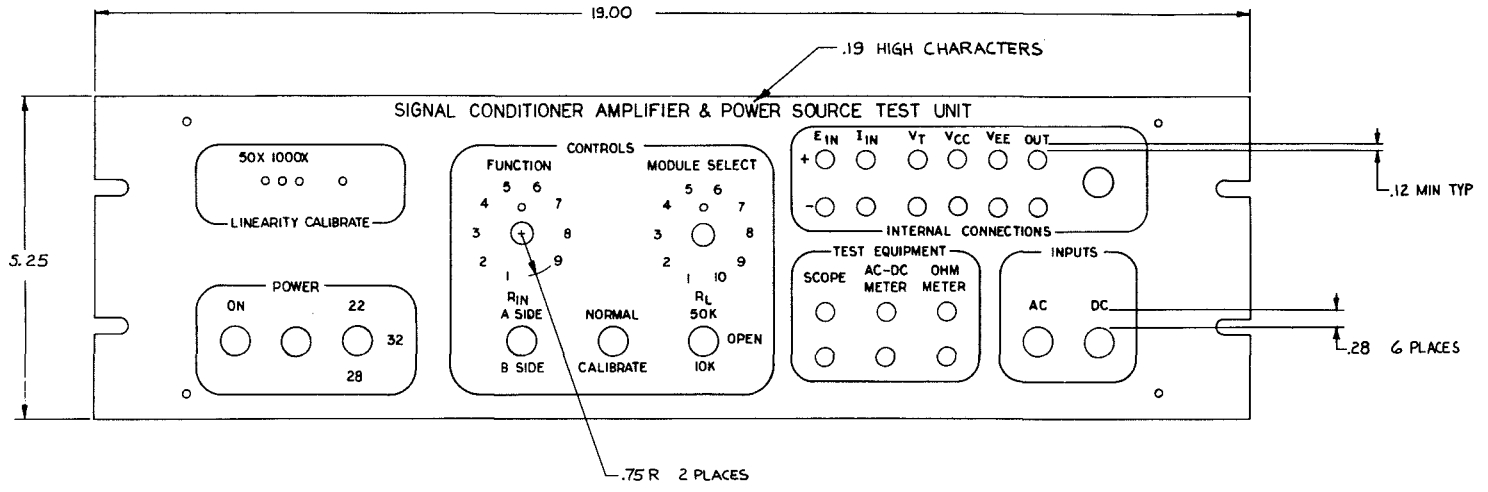


Figure 5-10. Test Unit, Front Panel

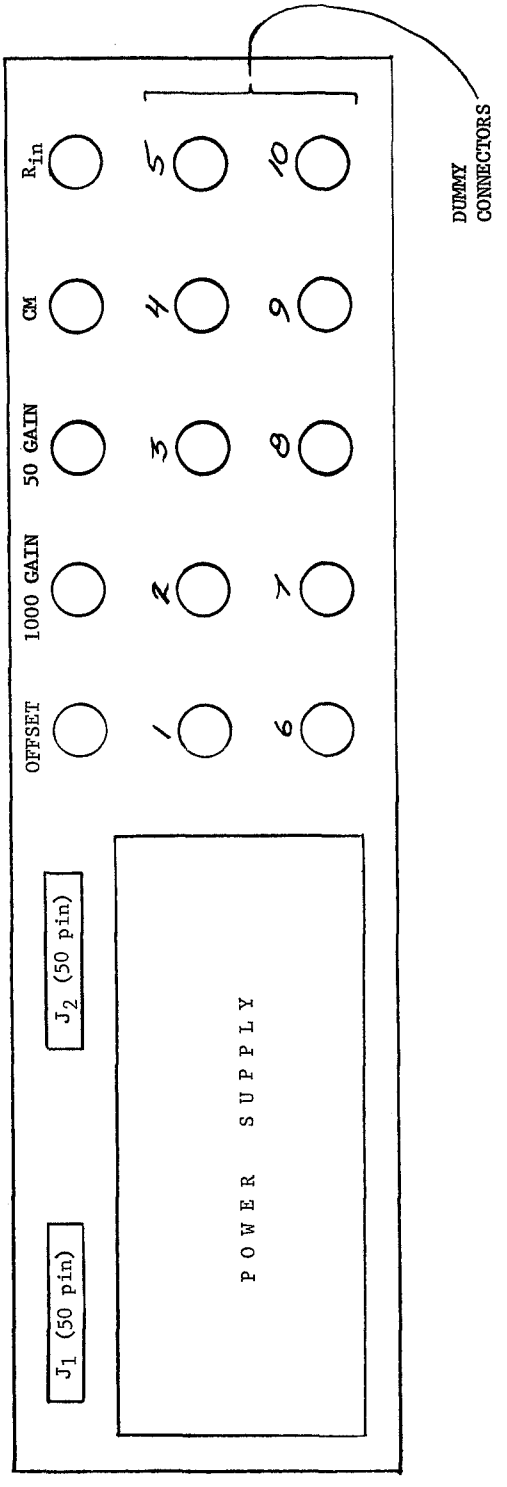
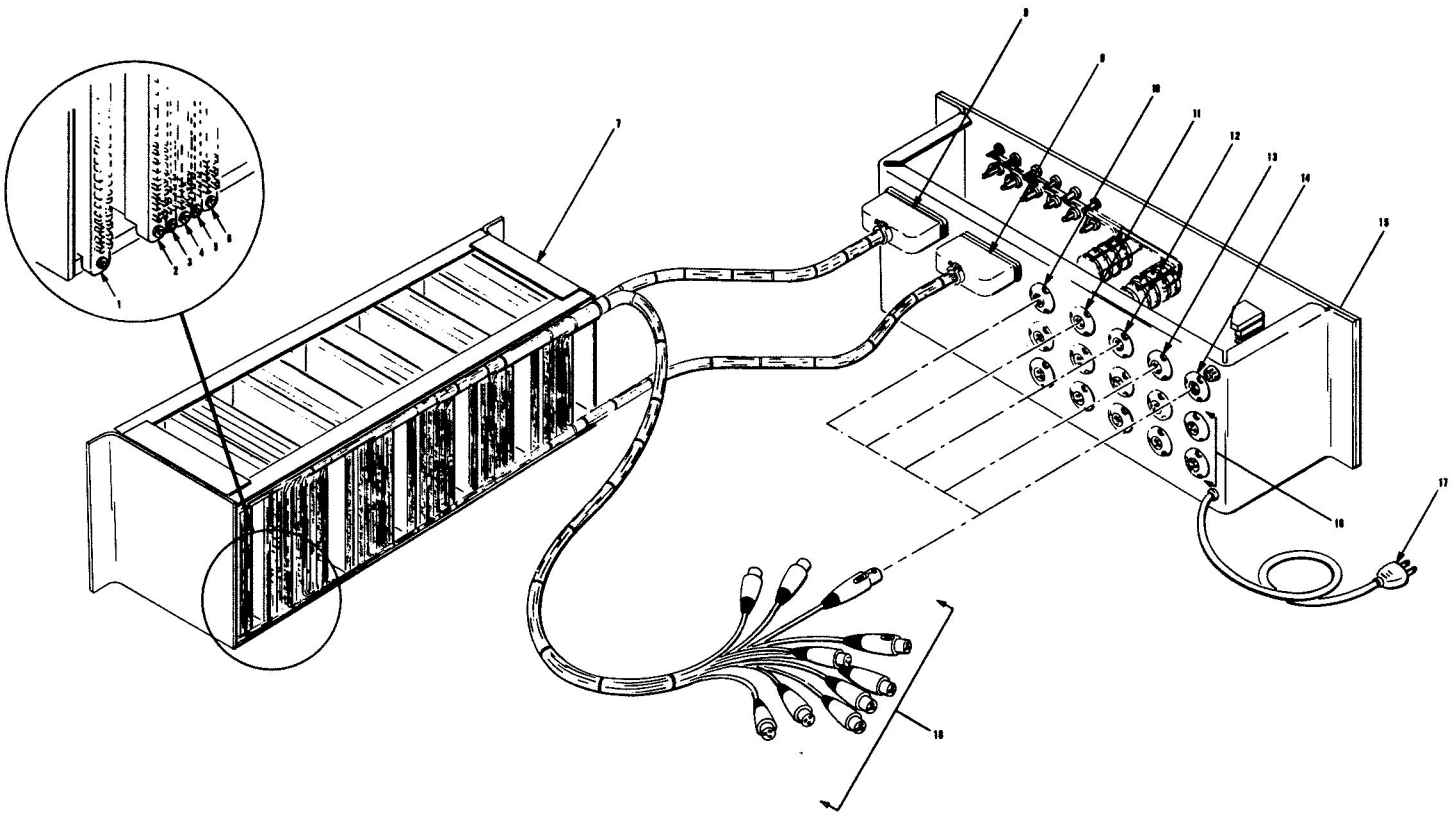


Figure 5-11. Test Unit, Rear View



1. Power Source
2. Extra Voltage Regulator
3. Differential Mode, Amplifier #1
4. Common Mode, Amplifier #1
5. Differential Mode, Amplifier #2
6. Common Mode, Amplifier #2
7. Card Cage
8. P2
9. P1
10. Z_{in}
11. Offset
12. 1000 Gain
13. 30 Gain
14. CM
15. Test Unit
16. Dummy Connectors
17. Power Cord
18. Amplifier Input Connectors

Figure 5-12. Test Set Connections

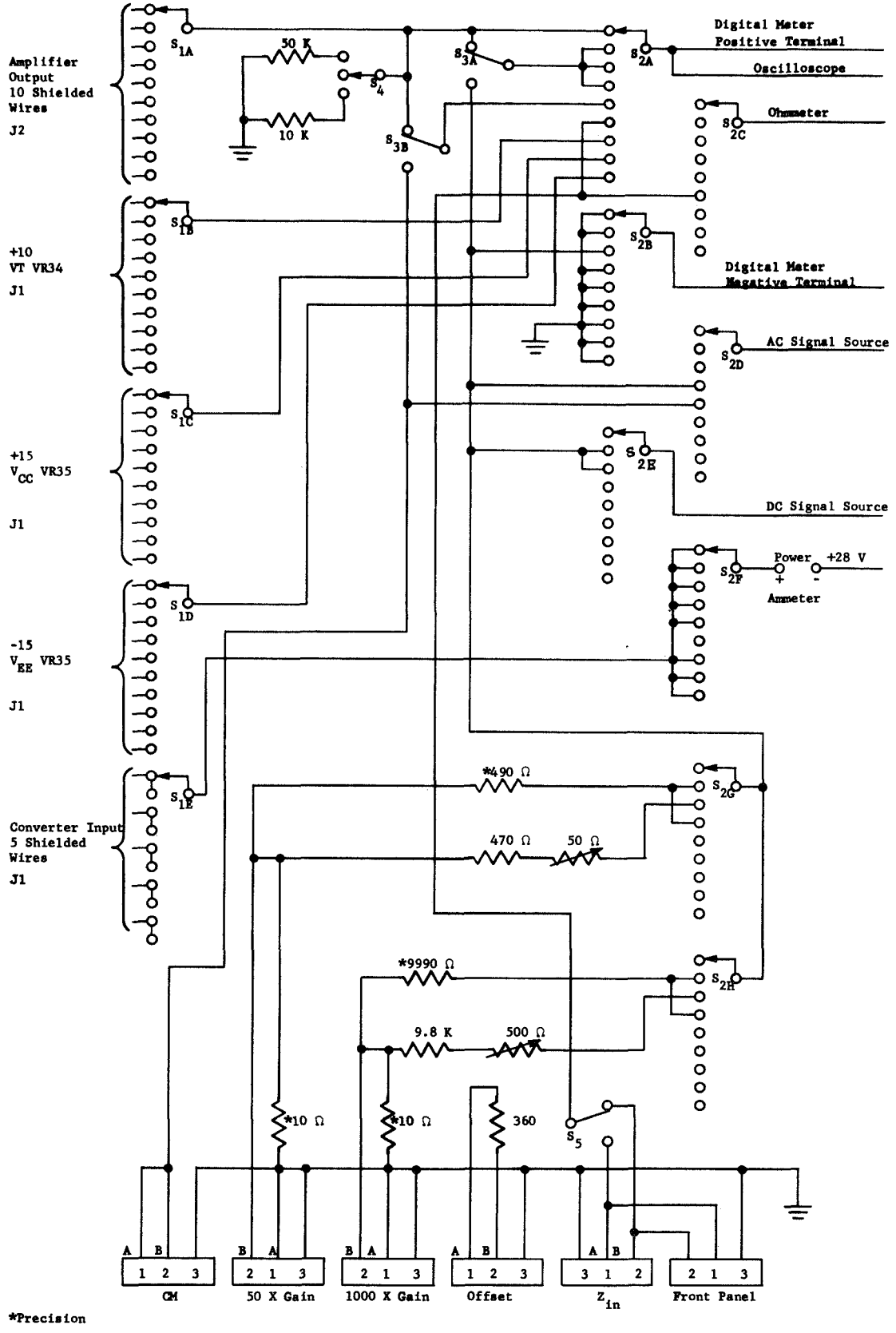


Figure 5-13. Test Set Wiring

4) Internal Connections - This section provides terminals for monitoring specific internal voltages. The E_{in} terminals monitor the input voltage to the power source. The I_{in} terminals monitor the voltage across a one-ohm resistor which is in series with the power source input. This allows measurement of the input current to the power source.

The following terminals are added for convenience and are not needed to conduct specification tests. The V_T terminals monitor the transducer excitation voltage. V_{CC} and V_{EE} terminals monitor the positive and negative amplifier supply voltages, respectively. The "Amp. Out" terminals monitor the output of the amplifier. The "Amp. In" connector provides access to the amplifier input when the shielded connector at the back of the test unit is inserted into the R_{in} receptacle.

5) Test Equipment - This section is used to connect the test unit to the measurement equipment. The suggested instruments are:

Oscilloscope:	Tektronix Model 545A, or equivalent, plus a preamp 25 mV per centimeter sensitivity and a 15 MHz bandwidth. (Tektronix CA or equivalent.)
AC-DC Meter:	Hewlett-Packard Model 2401 Dymec Integrating Digital Voltmeter with converter, or equivalent.
Ohmmeter:	Any ohmmeter which will measure 50 K to 100 K ohms within 10%.

6) Inputs - The test unit signal generators are connected into this section. The suggested instruments are:

DC Source:	Kitel Model 303, or equivalent.
AC Source:	Hewlett-Packard Model 202C, or equivalent.

5.3.2 Rear

The input of each of the ten amplifiers in the card file are connected to the test unit through individually shielded cable and connectors. Each

input connector is held in standby in the numbered row of mating connectors shown in Figure 5-10. (These mating connectors serve no electrical purpose, but provide orderly mechanical support for the unused amplifier input connectors.) The input connector of the amplifier to be measured is taken out of the numbered mating connector and inserted in one of the following mating connectors.

1) Offset: For amplifier output offset measurements.

2) 1000 Gain: For gain, linearity, and output impedance measurements for a gain of 1000 amplifier.

3) 50 Gain: For gain, linearity, and output impedance measurements for a gain of 50 amplifier.

4) CM: For common-mode rejection measurements.

5) R_{in}: For input impedance measurements.

All interconnections other than the amplifier inputs are made through two multi-pin connectors, as shown.

5.4 TEST PROCEDURE

Place the card file in a temperature controlled dehumidified chamber and connect it to the test unit. Connect the specified signal generators and test instruments to the test unit. Connect the test unit to 110 volt ac/60 Hz power with the ON-OFF switch in the OFF position. Start with the "Module Select" switch in position 1, the "Normal-Calibrate" switch in the Calibrate position, R_L set to 50 K, and the input voltage selected at +28 volts.

First, take all the measurements at room temperature, +25°C, then the appropriate measurements at -35°C, -10°C, +71°C, and +95°C (not all tests are made over the full range). Record all the data.

5.4.1 Amplifier Output Offset and Noise

1) Connect the input of amplifier #1 to the offset connector.

2) Turn ON the test unit and allow the modules to warm up for at least ten minutes.

3) Take a peak-to-peak noise measurement and record.

4) Read the DC Digital Meter and record the amplifier offset.

5) Set the input voltage to +22 volts and record the amplifier offset.

6) Set the input voltage to +32 volts and record the amplifier offset.

7) Turn the power off.

8) Set the "Module Select" switch to position #2.

9) Return the input of amplifier #1 to connector #1 and place the input of amplifier #2 into the offset connector.

10) Turn ON the test unit and allow the modules to warm up for at least ten minutes.

11) Take a peak-to-peak noise measurement and record.

12) Read the DC Digital Meter and record the amplifier offset.

13) Set the input voltage to +22 volts and record the amplifier offset.

14) Set the input voltage to +32 volts and record the amplifier offset.

15) Turn the power off.

16) Repeat the above for amplifiers #3 through #10.

5.4.2 Amplifier DC Gain - R_O

1) With the power off, set the "Module Select" switch to position #1 and the "Function" switch to position #2.

2) Insert the input of amplifier #1 into the 1000 gain connector. (NOTE: Amplifiers #1 through

#5 are a gain of 1000. Upon testing amplifiers #6 through #10, which are gain of 50, the inputs should be inserted into the 50 gain connectors.)

3) Set the "Normal-Calibrate" switch to Calibrate, the R_L switch to open, and the input voltage switch to +28.

4) Set the DC Signal Source to zero volts.

5) Turn ON the test unit and allow modules to warm up for at least 10 minutes.

6) Set the "Normal-Calibrate" switch to Normal.

7) Record the amplifier output voltage.

8) Set the "Normal-Calibrate" switch to Calibrate and set the Signal Source to +1.000 volt. Record the actual input voltage.

9) Set the "Normal-Calibrate" switch to Normal.

10) Record the amplofier output voltage.

11) Repeat above procedure for +3 volt, +4 volt, and +5 volt inputs.

12) With the input voltage set at +5.000 volts, switch R_L to 10 K.

13) Record the amplifier output voltage.

14) From the zero and full-scale five-volt input increments, calculate the amplifier dc gain and record.

15) From the measurements at one volt input increments, calculate the deviation from perfect linearity and record.

16) From the measurement of the full-scale output voltage, with open circuit and 10 K ohm load, calculate the output impedance as follows:

$$R_o = \frac{\Delta V}{5 \times 10^{-4}} \text{ ohms}$$

ΔV = change in full-scale output voltage from no load to 10 K ohm load, expressed in volts.

17) Turn power off.

18) Set "Module Select" switch and connect amplifier input appropriately and repeat all of above for amplifiers #2 through #10.

5.4.3 Linearity Measurements

1) With the power off, set the "Module Select" switch to position #1 and the "Function" switch to position #2.

2) Insert the input of amplifier #1 into the 1000 gain connector. (Note: Amplifiers #1 through #5 are a gain of 1000. Upon testing amplifiers #6 through #10, which are a gain of 50, the inputs should be inserted into the 50 gain connector.)

3) Set the DC Signal Source to zero volts.

4) Turn ON the test unit and allow modules to warm up for at least 10 minutes.

5) Read and record the DC Digital Meter reading.

6) Set the DC Signal Source to +5.0 volts.

7) Adjust the "Linearity Calibrate" control so that the DC Digital Meter reads the offset recorded in 5).

8) Set the DC Signal Source from -3 to +8 volts in one volt stops. Read and record meter reading in each case.

9) Subtract from each recorded reading the original offset reading. The result is the deviation from linearity.

5.4.4 Amplifier Frequency Response

1) With the power off, set the "Module Select" switch to position #1 and the "Function" switch to position #3.

2) Insert the input of amplifier #1 into the 1000 gain connector. (Note: Amplifiers #1 through #5 are a gain of 1000. Upon testing amplifiers #6 through #10, which are gain of 50, the inputs should be inserted into the 50-gain connectors.)

3) Set the "Normal-Calibrate" switch to Calibrate, the R_L switch to 50 K ohms, and the input voltage switch to +28.

4) Set the AC Signal Source to 2 volts peak-to-peak amplitude (0.707 V rms on AC Voltmeter), and 100 Hz.

5) Turn ON the test unit.

6) Set the "Normal-Calibrate" switch to Normal.

7) Record the amplifier output voltage.

8) Repeat steps #3 through #7 for frequencies of 0.2, 0.5, 1, 2, 5, 10, 20, 50, and 100 KHz.

9) Observing the oscilloscope, adjust the AC Signal Source for 1 KHz with an amplitude such that the amplifier limits in both the positive and negative directions. Record this limiting value.

10) Turn power off.

11) Set "Module Select" switch and connect amplifier input appropriately and repeat all of the above for amplifiers #2 through #10.

5.4.5 Amplifier Common-Mode Rejection

1) With the power off, set the "Module Select" switch to position #1 and the "Function" switch to position #4.

2) Insert the input of amplifier #1 into the CM connector.

3) Set the "Normal-Calibrate" switch to Calibrate, the R_L switch to 50 K ohms, and the input voltage switch to +28.

4) Set the AC Signal Source to 2 volts peak-to-peak amplitude, 100 Hz.

5) Turn ON the test unit.

6) Set the "Normal-Calibrate" switch to Normal.

7) Record the amplifier output voltage.

8) Repeat steps #3 through #7 for frequencies of 0.2, 0.5, 1, 2, 5, and 10 KHz.

9) Turn power off.

10) Set "Module Select" switch and connect amplifier input appropriately and repeat all of the above for amplifiers #2 through #10.

5.4.6 Amplifier Input Resistance

1) With the power off, set the "Module Select" switch to position #1 and the "Function" switch to position #5.

2) Insert the input of amplifier #1 into the R_{in} connector.

3) Set the R_{in} switch to A side and record resistance measurement.

4) Set the R_{in} switch to B side and record resistance measurement.

5) Repeat above stpes #1 through #4 for amplifiers #2 through #10.

5.4.7 Power Source Voltages

1) With the power off, set the "Module Select" switch to position #1 and the "Function" switch to position #6. Turn power on and allow the modules to warm up for at least 10 minutes.

2) Measure and record the peak-to-peak noise on the oscilloscope.

3) Measure and record the dc output voltage for +22, +28, and +32 volts input to the signal source.

4) Turn power off and repeat above steps #1 through #3 for positions 3, 5, 7, and 9. (Note: There are five power sources.)

5.5 TEST DATA

Following is a summary of the Signal Conditioning Module test data.

1) Output Offset (MV)

SN	-30°F	0°F	+75°F	+160°F	+200°F
301	+21	- 1	- 8	+ 8	+12
304	+50	+43	+21	+27	+32
315	+20	+ 4	-34	-20	-20
308	+24	+16	-12	+ 3	+ 7
319	-17	-17	-36	-22	-40
401	+18	+ 5	-11	+15	+23
402	- 8	+ 6	+26	+19	-22
406	-17	-18	+ 1	+ 6	+11
408	+ 9	+ 6	+ 2	+ 1	- 2
411	+ 5	- 2	-10	- 5	- 2

2) Output Peak-to-Peak Noise (MV)

SN	-30°F	0°F	+75°F	+160°F	+200°F
301	9	15	20	10	10
304	10	15	10	10	10
315	10	10	10	10	10
308	10	9	10	10	10
319	10	15	10	10	10
401	10	10	9	15	10
402	10	10	3	15	10
406	10	10	5	10	10
408	10	10	5	20	10
411	5	10	10	20	10

3) Actual Gain

SN	-30°F	0°F	+75°F	+160°F	+200°F
301	1004.2	1001.6	1000.6	999.6	999.2
304	990.0	989.0	987.8	988.6	987.4
315	1003.0	1002.4	1000.6	999.4	998.2
308	998.2	998.2	998.4	1000.6	999.4
319	1002.2	1002.4	1001.4	1000.4	999.0
401	50.18	50.16	50.20	50.24	50.26
402	49.89	49.90	49.95	49.92	49.93
406	50.03	50.09	50.10	50.13	50.15
408	49.96	50.00	50.03	50.07	50.10
411	49.89	49.90	49.91	49.90	49.93

4) Gain in Percent of Ideal

SN	-30°F	0°F	+75°F	+160°F	+200°F
301	+ .42%	+ .16%	+ .06%	- .04%	- .08%
304	-1.00%	-1.10%	-1.22%	-1.14%	-1.26%
315	+ .30%	+ .24%	+ .06%	- .06%	- .18%
308	- .18%	- .18%	- .16%	+ .06%	- .06%
319	+ .22%	+ .24%	+ .14%	+ .04%	- .01%
401	+ .36%	+ .32%	+ .40%	+ .48%	+ .52%
402	- .22%	- .20%	- .10%	- .16%	- .14%
406	+ .06%	+ .18%	+ .20%	+ .26%	+ .30%
408	- .08%	0%	+ .06%	+ .14%	+ .20%
411	- .22%	- .20%	- .18%	- .20%	- .14%

5) Gain in Percent of 75°F Value

SN	-30°F	0°F	+75°F	+160°F	+200°F
301	+.36%	+.10%	0%	-.10%	-.14%
304	+.22%	+.12%	0%	+.08%	-.04%
315	+.24%	+.18%	0%	-.12%	-.24%
308	-.02%	-.02%	0%	+.22%	+.10%
319	+.08%	+.10%	0%	-.10%	-.15%
401	-.04%	-.08%	0%	+.08%	+.12%
402	-.12%	-.10%	0%	-.06%	-.04%
406	-.14%	-.02%	0%	+.06%	+.10%
408	-.14%	-.06%	0%	+.08%	+.14%
411	-.04%	-.02%	0%	-.02%	+.04%

6) Output/Input Impedances (ohms)

SN	Output Impedance	Input Impedance
301	12	200 K
304	8	230 K
315	10	150 K
308	8	136 K
319	6	107 K
401	< 1	188 K
402	< 1	>200 K
406	2	136 K
408	< 1	137 K
411	20	146 K

7) Linearity (Deviation from Linearity in mV)

SN	-3	-2	-1	0	1	2	3	4	5	6
301	+1	+1	+1	0	+1	+1	+1	+1	0	0
304	+1	+1	+1	0	0	+1	0	0	0	-1
315		0	0	0	0	+1	+1	+1	+1	+1
308	-11	-8	-6	0	+1	+3	+6	+8	+1	-7
319	-1	-1	-1	0	0	0	0	0	0	-1
401	-1	-1	0	0	0	0	+1	+1	+2	+3
402		-2	-2	0	+1	+1	+2	+3	+3	+4
406	+1	0	0	0	0	0	-1	-1	0	0
408	0	+2	0	0	0	0	0	0	0	0
411	+2	0	0	0	0	+1	+1	+1	+1	+2

8) Frequency Response Referenced to 100Hz Gain (%)

SN	200~	500~	1KHz	2KHz	5KHz	10KHz	20KHz	50KHz	100KHz
301	-0.3	-0.8	-2.4	-7.9	-30.5	-56.5	-77.1	-92.1	-96.4
304	+0.6	0	-1.9	-8.6	-33.7	-60.4	-79.6	-93.5	-97.3
315	-0.1	-0.3	-1.4	-5.8	-25.9	-51.9	-73.8	-90.4	-96.3
308	+0.4	0	-1.4	-6.0	-26.6	-52.4	-73.9	-90.2	-91.1
319	0	0	-0.7	-3.1	-16.2	-39.4	-64.0	-85.8	-93.6
401	+0.2	0	-0.8	-3.0	-15.6	-38.6	-65.4	-87.5	-94.0
402	0	0	-1.2	-3.0	-14.8	-36.6	-62.6	-86.7	-93.6
406	0	-0.4	-0.8	-2.2	-13.8	-35.2	-60.6	-84.0	-92.5
408	-0.2	-0.4	-1.0	-3.8	-16.2	-38.6	-63.6	-85.0	-92.8
411	0	-0.4	-0.8	-2.8	-13.8	-35.6	-61.0	-84.9	-93.2

9) Common-Mode Rejection (dB)

SN	100~	200~	500~	1KHz	2KHz	5KHz	10KHz
301	98	98	98	98	98	97	92
304	118	112	107	103	97	91	89
315	115	118	115	118	115	112	104
308	109	109	112	110	106	100	98
319	112	112	118	115	112	106	103
401	103	103	106	100	92	86	73
402	84	84	83	84	84	84	82
406	78	78	78	76	72	65	62
408	103	100	95	90	84	78	75
411	104	100	97	92	86	79	77

10) Power Supply Measurements, SN-63, DC Out Error (mV)

Temp. °F	22 Volts In Volts			28 Volts In Volts			32 Volts In Volts			Ripple P-P on 10V
	+10	+15	-15	+10	+15	-15	+10	+15	-15	28V in
-30	+25	-57	-72	+28	-56	-75	+32	-54	-78	60
0	+18	-36	-51	+21	-33	-53	+24	-33	-56	44
+75	+ 3	+19	+ 7	+ 5	+22	+ 4	+ 7	+24	+ 3	24
+160	-11	+46	+31	- 9	+47	+31	- 8	+48	+28	30
+200	-25	+55	-11	-24	+58	-13	-22	+58	-13	44

11) Power Supply Measurements, SN-965, DC Out Error (mV)

Temp. °F	22 Volts In Volts			28 Volts In Volts			32 Volts In Volts			Ripple P-P on 10V
	+10	+15	-15	+10	+15	-15	+10	+15	-15	28V in
-30	+21	- 7	+17	+28	- 6	+17	+28	- 4	+14	50
0	+18	+ 1	+13	+26	+ 2	+11	+24	+ 4	+ 8	48
+75	+14	+13	0	+14	+14	- 1	+14	+14	- 3	44
+160	- 4	+12	- 3	- 4	+13	- 3	- 2	+13	- 5	60
+200	-10	+ 7	- 1	-11	+40	-38	- 9	+ 9	- 4	50

12) Power Supply Measurements, SN-966, DC Out Error (mV)

Temp. °F	22 Volts In			28 Volts In			32 Volts In			Ripple P-P on 10V
	Volts			Volts			Volts			
	+10	+15	-15	+10	+15	-15	+10	+15	-15	28V in
-30	- 9	+14	-18	- 8	+19	-19	- 4	+25	-21	60
0	- 7	+10	-19	- 6	+15	-21	- 2	+21	-23	46
+75	- 3	- 1	-19	- 3	+ 1	-21	- 1	+ 5	-22	60
+160	- 3	-20	-14	- 3	-18	-15	- 1	-16	-15	38
+200	- 5	-28	- 8	- 4	-26	- 8	- 3	-24	- 9	66

13) Power Supply Measurements, SN-968, DC Out Error (mV)

Temp. °F	22 Volts In			28 Volts In			32 Volts In			Ripple P-P on 10V
	Volts			Volts			Volts			
	+10	+15	-15	+10	+15	-15	+10	+15	-15	28V in
-30	+20	+35	+35	+22	+37	+34	+24	+38	+34	54
0	+12	+35	+33	+12	+37	+33	+10	+37	+31	36
+75	- 4	+14	+31	- 2	+16	+31	- 1	+17	+30	20
+160	-12	-30	+41	-13	-28	+41	-13	-27	+40	52
+200	-18	-51	+49	-17	-50	+48	-16	-49	+47	42

14) Power Supply Measurements, SN-967, DC Out Error (mV)

Temp. °F	22 Volts In			28 Volts In			32 Volts In			Ripple P-P on 10V
	Volts			Volts			Volts			
	+10	+15	-15	+10	+15	-15	+10	+15	-15	28V in
-30	+30	-11	+42	+31	-10	+41	+31	- 9	+40	45
0	+23	- 5	+31	+24	- 4	+28	+26	- 4	+28	45
+75	+ 6	+ 6	- 1	+ 6	+ 6	- 2	+ 7	+ 8	- 2	43
+160	-14	+10	- 9	-13	+11	- 9	-13	+12	-11	47
+200	-28	+ 4	+13	-27	+ 5	+13	-26	+ 5	+12	45

6. CONCLUSIONS AND RECOMMENDATIONS

This contract successfully demonstrated the following points:

a) The amplifier electrical specifications were fully met over the full temperature range. This direct-coupled monolithic amplifier can therefore be used in many applications presently requiring chopper amplifiers.

b) This amplifier development is ready to be transferred into small-scale production. The recommended follow-on effort is to fabricate forty or more amplifiers to thoroughly test and evaluate, thereby providing the needed transfer into small-scale production quantities. This phase is necessary to reduce the selling cost of the amplifier, making it cost competitive with present-day discrete component chopper amplifiers.

c) The microminiature power source met all line, load, and temperature regulation specifications.

d) Recommended follow-on effort of the power source includes improving the high frequency spike RFI performance and reviewing the mechanical package design for decreased cost and increased reliability. Further attention is also appropriate to increase the power efficiency (presently 40%). This can be accomplished by applying negative feedback around the converter. The significantly improved converter regulation characteristics would then allow the series regulators to be removed (new efficiency 70%).

APPENDIX A

CONTRACT PERFORMANCE SPECIFICATIONS

NOTE: Numbering used on the following specifications is taken directly from the contract.

4.0 MISCELLANEOUS

4.1 Battery. The power supply shall be powered from an external battery. The characteristics of this battery are as follows:

4.1.1 The voltage is between 22 and 32 volts with 28 volts being nominal.

4.1.2 There is a possible maximum 4 volt peak-to-peak ripple (dc to 2 square wave) impressed upon the battery voltage. The battery voltage, including the ripple, will be between 22 and 32 volts.

4.1.3 There is a possible transient on the power line that may reduce the battery voltage to as low as 0 volts or increase it to as high as 42 volts. This transient has a 20 millisecond base width duration and an 8 millisecond rise time. The circuitry connected to the battery is required to survive this transient, but the specification performance is not required. Operation shall return to normal within 100 microseconds after the duration of the pulse.

4.2 Service Life. The modules shall be capable of operation within specifications for a minimum of 2000 hours, continuously or otherwise, during a service life of one year.

4.3 Warm-Up Time. The modules shall be capable of operation within specifications after a warm-up time not to exceed 0.5 minute.

4.4 Color. The module cases shall be opaque.

4.5 Reverse Polarity Protection. All modules connected to the battery shall be protected from being destructed by polarity reversal. operation shall return to normal with proper polarity connections.

4.6 Product Marking. The modules and all external leads shall be marked for identification purposes in a permanent manner.

4.7 Workmanship. Uniformity of shapes, dimensions, and performance shall provide interchangeability of the complete moduels.

5.0 PERFORMANCE SPECIFICATIONS

5.1 DC-to-DC Power Converter. The module shall be designed to operate from the battery described in Para. 4.1 and provide the power to two regulator modules described by Para. 5.3 within the specifications of performance.

5.1.1 Volume. The module shall be rectilinear. The volume shall not exceed 0.80 cubic inches.

5.1.2 Isolation. The module shall be designed so that the output circuit shall be transformer-isolated from the input circuit.

5.1.3 Efficiency. The module shall be designed with efficiency considerations equal in importance to the other specification requirements.

5.1.4 Voltage and Current. The module shall be designed to provide the proper voltages and currents to power the two regulators described in Para. 5.3.

5.1.5 Regulation and Stability. The module shall be designed to properly power, at the same environment, the two regulators described in Para. 5.3.

5.1.6 Power Line Feedback. The feedback ripple from the module to the battery shall be no more than 30 mV peak-to-peak as measured across a one-ohm series resistor with an oscilloscope having a pass band of 15 MHz.

5.1.7 Ripple. The ripple on the output voltages shall be of such value that the regulators will operate the amplifiers and transducers within their respective ripple specifications (Para. 5.2.9 and 5.3.1.3).

5.1.8 Mounting Considerations. The external leads shall be in a plane parallel to the flat bottom surface and located in a predetermined precise manner. These leads shall be bare bus bar of such material suitable for retaining the module to a printed circuit board for operation in the specified environments.

5.2 DIFFERENTIAL DC AMPLIFIER
The module shall be powered from the voltage regulator described in Para. 5.3.

5.2.1 Input Signal. The module shall be capable of receiving variable differential input signals from 0 to +5 volts. Those signals too large for linear amplification shall not damage the amplifier.

5.2.2 Input Circuit. The module shall not require the signal source to provide bias current.

5.2.3 Input Impedance. The module shall have an input impedance of no less than 50 K ohms for an input signal of any frequency between dc and 1 KHz. The source impedance, as seen by the module, is 0 to 375 ohms differential.

5.2.4 Output Signal. The module shall be capable of delivering output signals of from 0 to +5 volts to a load variable from 50 K ohms to an open circuit.

5.2.5 Output Impedance. The output impedance of the module shall not exceed 100 ohms from dc to 1 KHz.

5.2.6 Output Offset. With a zero input signal from a source impedance as specified, the module output voltage shall be 0 ± 50 millivolts.

5.2.7 Voltage Gain. The voltage gain shall be within 1% of the ideal value of 50 for the -1 amplifier and 1000 for the -4 amplifier.

5.2.8 Gain Stability and Frequency Response. The gain of the module shall be within ± 1% of the dc value at 75° from dc to 1 KHz. The 3 dB point shall not exceed 15 KHz. The frequency response between dc and 1 KHz shall not change more than ± 1% over the specified environments.

5.2.9 Output Ripple. The maximum output ripple voltage shall be 25 millivolts peak-to-peak as measured with an oscilloscope having a pass band of 15 megacycles.

5.2.10 Linearity. The module shall have a linear output within ±12.5 millivolts of a straight line between the output end points (nominal 0 and +5 volts).

5.2.11 Common Mode. The module shall have a common mode rejection ratio of 80 dB or more for frequencies from dc to 1 KHz and voltages of ± 1.0 volts.

5.2.12 Volume. The module shall be constructed in a rectilinear configuration with a volume not to exceed 00.01 cubic inches.

5.2.13 Mounting Considerations. The external leads shall be brought out of the module from two opposing surfaces and in one plane. These leads shall be bare bus bar of such material suitable for retaining the module to a printed circuit board for operation in the specified environments.

5.3 VOLTAGE REGULATOR

The module shall be designed to receive power from the dc-to-dc Power Converter described in Para. 5.1 and deliver regulated power to one external transducer and one external amplifier.

5.3.1 Transducer Power Specifications

5.3.1.1 Voltage and Current. The module shall be designed to deliver 10 volts to one 350 ± 5% ohm transducer.

5.3.1.2 Regulation and Stability. The voltage shall be 10 volts dc ± 50 millivolts when connected to a typical transducer and subjected to the battery fluctuations and the specified environments.

5.3.1.3 Ripple. The ripple on the 10 volts shall not exceed 25 millivolts peak-to-peak as measured with an oscilloscope having a pass band of 15 megahertz.

5.3.2 Amplifier Power Specifications.

5.3.2.1 Voltage and Current. The module shall be designed to provide the proper voltages and currents to power one amplifier for the performance described by Para. 5.2.

5.3.2.2 Regulation and Stability. The module shall be designed to properly power, at the same environment, one amplifier for the performance described in Para. 5.2.

5.3.2.3 Ripple. The ripple on the supply voltages shall be of such value that the ripple of the amplifier output (Para. 5.2.9) is within specifications.

5.3.3 Mounting Considerations. The external leads shall be in a plane parallel to the flat bottom surface and located in a predetermined precise manner. These leads shall be bare bus bar of such material suitable for retaining the module to a printed circuit board for operation in the specified environments.

APPENDIX B

SPECIFICATIONS OF SINGLE DIE BASIC AMPLIFIER

General Description

The MIA-101 is a direct coupled, high gain amplifier with a differential input and single ended output capability. The device is a one die compatible monolithic integrated circuit incorporating a buried layer epitaxial substrate with evaporated cermet thin film resistors. It features a high gain common-mode feedback loop which provides the flexibility of using either overall base feedback or emitter feedback. The latter option allows the amplifier to be used in high gain, low drift, high common-mode rejection applications. The MIA-101 can be used as an operational amplifier, a low-level instrumentation amplifier, linear or nonlinear function generator, and other applications requiring a high differential open loop voltage gain amplifier.

Absolute Maximum Ratings

Supply Voltages	$\pm$ 16 volts
Internal Power Dissipation	250 mW
Differential Input Voltage	$\pm$ 5 volts
Input Voltage	+7 to -4 volts
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C

Electrical Characteristics

(Nominally $T_A = +25^oC$ and $V_{cc} = V_{EE} = 15$ volts)

	Min.	Typical	Max.	Units
Input Offset Voltage		1.5	3	mV
Input Offset Voltage Temp. Coef. @-35°C to 95°C		3	6	μV/°C
Input Offset Current		20		nA
Input Offset Current @ -35°C			100	nA
Input Bias Current		100		nA
Input Bias Current @ -35°C			250	nA
Differential Input Resistance, Open-Loop		250		KΩ
Differential Input Resistance, Emitter Feedback Closed Loop		250T		KΩ
Common-Mode Input Resistance		200		MΩ
Common-Mode Input Voltage	-4		+7	volts
Common-Mode Rejection Ratio		100		dB
Supply Voltage Rejection Ratio		20		μV/volt
Voltage Gain, Open-Loop		110		dB
Voltage Gain Temperature Coefficient, Open-Loop @ -35°C to +95°C		0.1		dB/°C
Output Voltage Swing @ R_L = 50 K	-5		+8	volts
Output Resistance, Open-Loop		100		Ω
Negative Power Supply Voltage (V_{EE})		15		volts
Positive Power Supply Voltage (V_{CC})		15	volts	
Power Consumption		135		mW

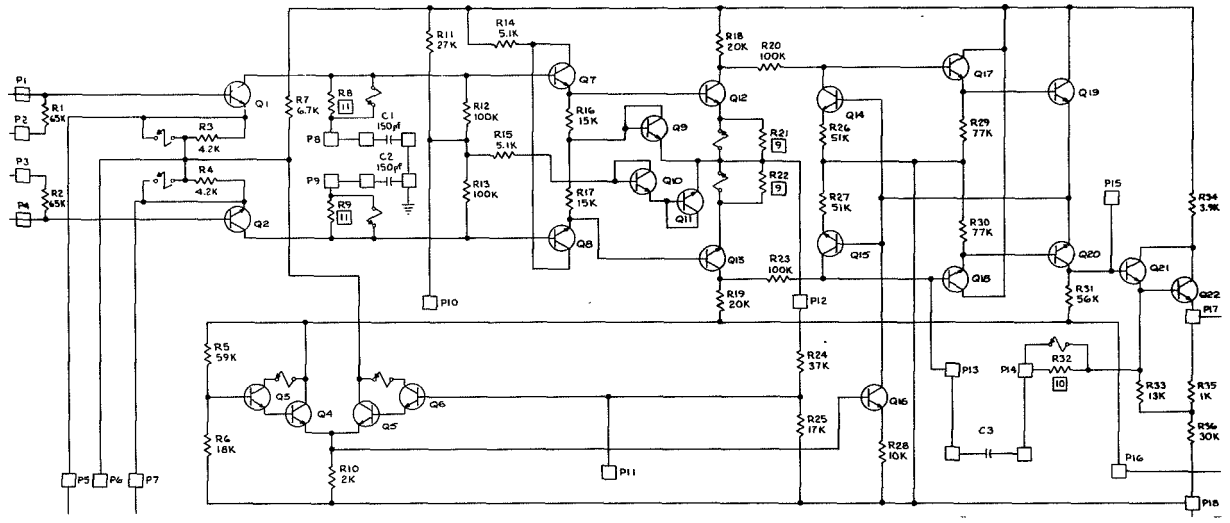


Figure B-1. MIA-101 Schematic

Definitions

$$T = \frac{\text{Open-loop Gain}}{\text{Closed-loop Gain}} + 1$$

Input Offset Voltage — Voltage applied to input terminals with a source resistance less than 10 ohms to obtain a zero output voltage.

Input Offset Current — Difference in the currents demanded at the two input terminals.

Input Bias Current — Average of the two input currents.

Differential Input Resistance — Dynamic resistance between input terminals.

Common-Mode Input Resistance — With the inputs shorted, the dynamic resistance from the inputs to ground

Common-Mode Input Voltage — Common-mode voltage limits in which the amplifier will perform linearily.

Common-mode Rejection Ratio — Ratio of the input voltage range to the maximum change in input offset voltage over this range.

Supply Voltage Rejection Ratio — Ratio of the change in input offset voltage to the change in supply voltage producing it.

Voltage Gain — Ratio of the change in output voltage to the change in voltage between the input terminals producing it.

Output Voltage Swing — Output voltage referenced to ground that can be obtained without clipping.

Output Resistance — Resistance between the output and ground with the output voltage at ground.

Power Consumption — DC power into the amplifier with the output voltage at ground and with no load current.

APPENDIX C

APPLICATION NOTES ON THE TRW MIA-101 MONOLITHIC AMPLIFIER

I. General Discussion

The MIA-101 is a direct coupled, high gain amplifier with a differential input and single-ended output capability. The device is a one die compatible monolithic integrated circuit incorporating a buried layer epitaxial substrate with evaporated cermet thin film resistors. It features a high gain common-mode feedback loop which provides the flexibility of using either overall base feedback or emitter feedback. The latter option allows the amplifier to be used in high gain, low drift, high common-mode rejection applications. The MIA-101 can be used as an operational amplifier, a low-level instrumentation amplifier, linear or nonlinear function generator, and other applications requiring a high differential open loop voltage gain amplifier.

The equivalent input voltage thermal drift of the MIA-101 is low and exceptionally linear. This characteristic, in addition to the emitter feedback feature, allows it to be used in low drift instrumentation amplifier applications. Ultra low drift (0.2 $\mu V/^{o}C$) and low offset (10μV) can be obtained over the full temperature range by adding a DOC-101 drift-offset control circuit which directly compensates the linear inherent amplifier thermal drift.

II. Fundamental DC Considerations

One of the primary features of the MIA-101 monolithic amplifier is the high gain common-mode feedback loop which stabilizes the common-mode collector currents of the input stage. This internal feedback feature allows equivalent input voltage differentials to be produced across the input stage emitters (as the current through R_{1A}-R_{1B} produces in Fig. C-1) without disturbing the bias conditions of the input stage. This provides a means for using overall emitter feedback in a high performance closed loop

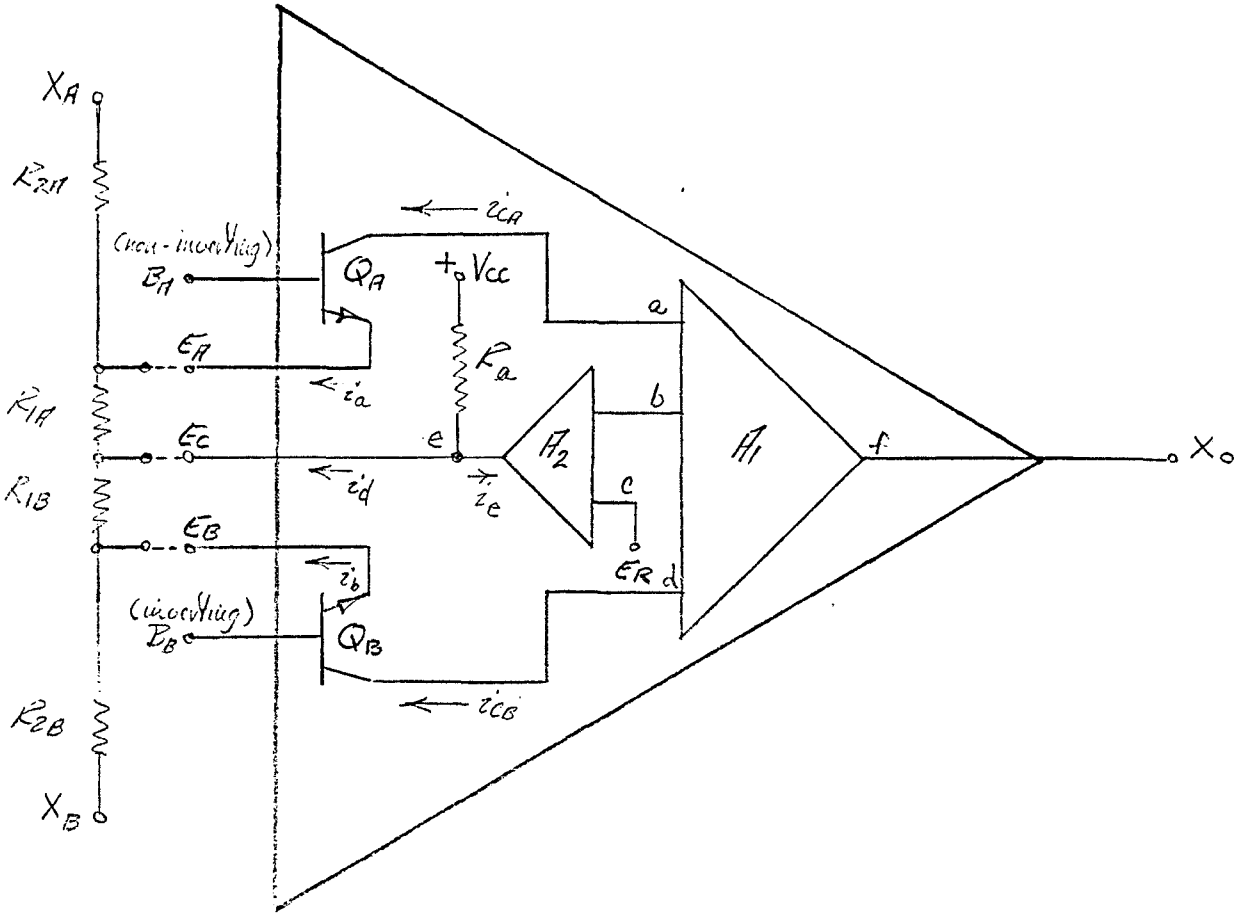


Figure C-1. TRW Monolithic Instrumentation Amplifier Block Diagram

amplifier application or for accurately comparing two independent differential signals at the input of one amplifier.

In Fig. C-1 the common-mode collector currents of $Q_A \cdot Q_B$, given by

$$i_c \equiv \frac{i_{cA} + i_{cB}}{2} \tag{1}$$

are converted into a voltage by amplifier section A_1 (point b) and compared by amplifier section A_2 with the reference voltage E_R (point c) to produce a current at E_C which adjusts itself to keep i_c constant. Resistor R_a is included on the die to provide positive i_d current into the external resistor network, since amplifier section A_2 is an NPN current sink. Varying common-mode voltages at $B_A \cdot B_B$ and/or $X_A \cdot X_B$ will cause changes in i_e. The stability afforded by the common-mode feedback loop is given by

$$\frac{\Delta i_e}{\Delta i_c} > 60 \text{ dB} \tag{2}$$

where Δi_e can be calculated as a function of common-mode voltage changes at $B_A \cdot B_B$ and/or $X_A \cdot X_B$, by

$$\Delta i_e \simeq \Delta \left(\frac{V_{B_A} + V_{B_B}}{2} \right) \times \left[R_{2A} \| R_{2B} \| (R_{1A} \| R_{1B} + R_a) \right] + \Delta V_{X_A} \times R_{2A} + \Delta V_{X_B} \times R_{2B} \tag{3}$$

Circuit parameters include:

$$i_c = 10 \ \mu A \tag{4}$$

$$i_e \text{ (max)} = 1500 \ \mu A \tag{5}$$

$$R_a = 6.7 \text{ K ohms} \tag{6}$$

With respect to dc common-mode biasing, the following two limiting conditions should be considered in application of the MIA-101.

1. Combination of

   a. Maximum negative common-mode voltage at the bases $B_A \cdot B_B$, and

   b. Maximum positive common-mode voltage at inputs $X_A \cdot X_B$.

   is determined by the maximum current which can be provided by R_a, considering that the correction current i_e approaches zero.

2. Combination of

   a. Maximum positive common-mode voltage at the bases $B_A \cdot B_B$, and

   b. Maximum negative common mode voltage at inputs $X_A \cdot X_B$

   is determined by the maximum current i_e which can be demanded by amplifier section A_2. A 1500μA maximum i_e should be used.

Amplifier section A_2 differentially amplifies the currents from Q_A and Q_B to produce a low impedance single-ended output voltage at X_o. The differential to single-ended gain (from $B_A \cdot B_B$ to X_o) is nominally:

$$A_o = 110 \text{ dB} \Big| \begin{array}{l} \\ @\ +25^{\circ}C \\ @\ (R_{1A} = R_{1B}) \ll (r_{E_A} = r_{E_B}) \end{array} \tag{7}$$

assuming that R_{1A} and R_{1B} are small compared to the emitter diffusion resistance values of the input stage,

$$r_{E_A} \simeq r_{E_B} = \frac{KT}{q\ I_E} \simeq 2600 \text{ ohms} \Big| \begin{array}{l} \\ @\ +25^{\circ}C \\ @\ I_E = 10\mu A \end{array} \tag{8}$$

External resistors R_{1A} and R_{1B} affect the open-loop voltage gain by

$$A_o' = A_o \times \frac{2600}{2600 + R_1} \tag{9}$$

where $$R_1 = R_{1A} \simeq R_{1B} \tag{10}$$

III. Basic Amplifier

Operational base feedback can be applied to most commercially available monolithic amplifiers if the amplifier can be frequency compensated to avoid oscillations. Emitter feedback can be applied only to those amplifiers that have been specifically designed for that application, such as the TRW MIA-101 monolithic device. Table C-I compares some of the important properties of base and emitter feedback.

TABLE C-I

EMITTER FEEDBACK AND BASE FEEDBACK COMPARISONS

	Property	Emitter Feedback	Base Feedback
1.	DC offset drift.	Offers much lower drifts, particularly for high gain applications.	Drift is large due to the amplifier input currents following through the large feedback resistors.
2.	Input Impedance.	Exceptionally high, not dependent on feedback resistors.	Limited by value of feedback resistor.
3.	Closed loop gain vs. source dependence.	Source impedance has second order effect on open loop gain, therefore has a near negligible effect on closed loop gain.	Source impedance affects the closed loop gain directly.
4.	Closed loop gain vs. feedback resistor dependence.	Closed loop gain is not determined by a simple ratio of impedances.	Closed loop gain is determined by a simple ratio of impedances.

A. Closed Loop Emitter Feedback Configuration

Fig. C-2 illustrates the MIA-101 used in a closed loop, emitter feedback, instrumentation amplifier configuration. Conventional operational feedback to the input bases is often unacceptable for applications requiring high input impedance, high closed-loop gain, and low dc drift. Emitter feedback can be used effectively in these applications.

Assuming amplifier symmetry and feedback-resistor symmetry such that

$$R_{iA} = R_{1B} = R_1, \text{ and} \tag{11}$$

$$R_{2A} = R_{2B} = R_2, \tag{12}$$

the closed loop gain equation can be written as

$$\frac{v_o}{v_{iA} - v_{iB}} = \left[\frac{R_1 + R_2}{R_1}\right] x \left[\frac{1}{1 - \frac{1}{A_o}\left(\frac{R_1 + R_2}{R_1} + \frac{R_2}{R_E}\right)}\right] \tag{13}$$

where $$R_E \equiv \frac{KT}{q\, I_E} + \frac{R_S + r'_B}{\beta} \tag{14}$$

$$A_o \equiv \text{Total differential input to single-ended output open-loop gain} \tag{15}$$

If A_o is very large, the closed loop gain becomes

$$\frac{v_o}{v_{iA} - v_{iB}} = \frac{R_1 + R_2}{R_1}, \left(\text{or } \frac{Z_1 + Z_2}{Z_1}\right) \tag{16}$$

Note that the closed loop gain is not the simple ratio of two impedances. Also, Z_1 must pass dc current.

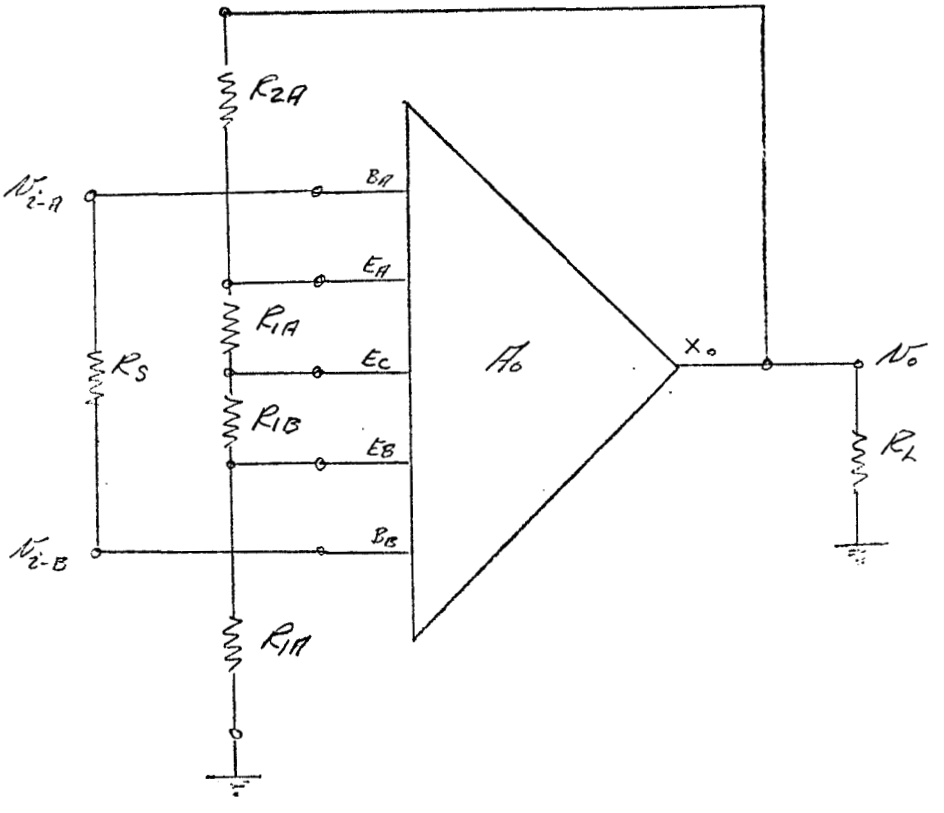


Figure C-2. Closed Loop Configuration with Emitter Feedback

For nonnegligible A_o, the closed loop voltage gain expressed by Equation 13 deviates from the ideal gain expressed by Equation 16 by the following percentage error.

$$\left(\%\ \text{error in}\ \frac{v_o}{v_{iA} - v_{iB}}\right) = \frac{1}{A_o} \times \left[\frac{R_1 + R_2}{R_1} + \frac{R_2}{R_E}\right] \tag{17}$$

It is important to note that the source impedance R_{S_1} affects the closed loop gain only as it affects A_o and R_E, which is not the case for operational base feedback.

Closed loop emitter feedback inherently provides high input impedance and low output impedance. From standard feedback analysis, the input impedance is given as

$$Z_{iF} = Z_i\ (T + 1) \tag{18}$$

where $$T \equiv \frac{\text{open loop gain}}{\text{closed loop gain}} + 1 \simeq \frac{A_o\ R_1}{R_1 + R_2} \tag{19}$$

$$Z_{iF} \equiv \text{input impedance with overall feedback} \tag{20}$$

$$Z_i \equiv \text{input impedance without overall feedback} \tag{21}$$

Also, from standard feedback analysis, the output impedance is given as

$$Z_{of} = \frac{Z_o}{T + 1} \tag{22}$$

where $$Z_{of} \equiv \text{output impedance with overall feedback} \tag{23}$$

$$Z_o \equiv \text{output impedance without overall feedback} \tag{24}$$

A distinct advantage of emitter feedback is the feature that the nonlinear temperature dependent input currents flow only through the source impedance. High closed gains, together with high input impedance can therefore be simultaneously obtained without the input current drift becoming intolerably large. The input current drift is not a function of the feedback impedances.

DC offset correction can be obtained by connecting resistor R_{1A} to a correction voltage, as shown in Fig. C-3. The amplifier output voltage will follow E_C.

Fig. C-4 shows an effective technique for correcting inherent offset and thermal drift with current sources which have been appropriately adjusted to demand the proper temperature-independent and temperature-dependent currents. This function can be obtained by using the DOC-101 monolithic integrated circuit with resultant equivalent input drifts less than $0.2\mu V/^{o}C$.

B. Closed Loop, Base Feedback Configuration

Fig. C-5 illustrates the MIA-101 used in a closed loop, base feedback, operational amplifier configuration. There is considerable literature on the basic principles of operational feedback. For brevity, therefore, this information is not included.

C. Open Loop, Dual-Differential Input Configuration

The MIA-101 amplifier can be uniquely used to perform the function shown in block form in Fig. C-6(a) by connecting the monolithic amplifier as shown in Fig. C-6(b). This application features the precise summing of multiple differential inputs at the input stage, thereby eliminating the need of any closed loop summing preamplifiers. This configuration is useful for

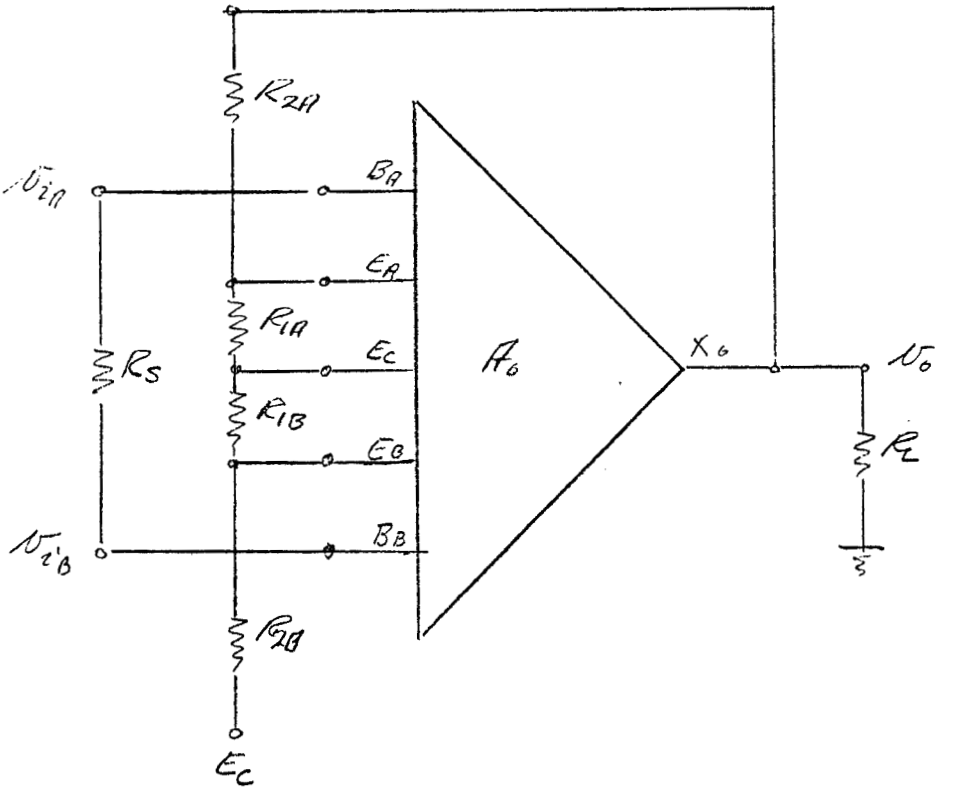


Figure C-3. Emitter Feedback With Offset Correction Voltage Source

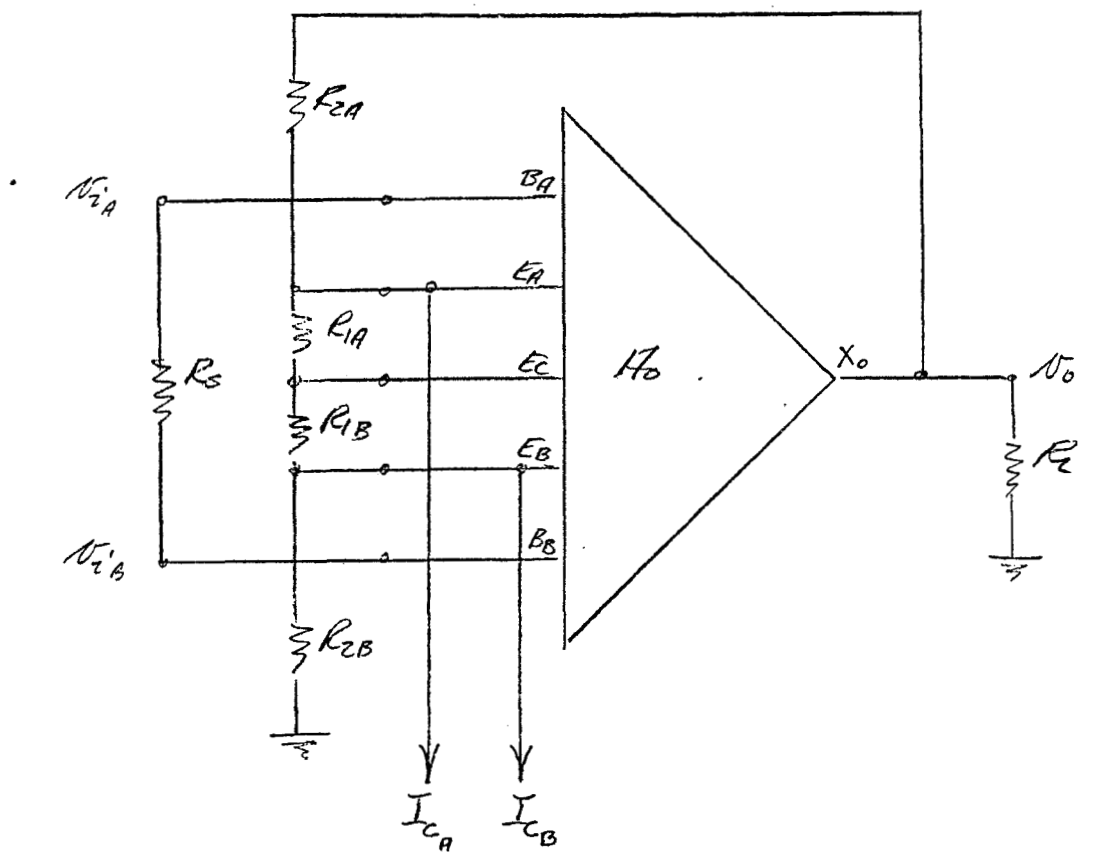


Figure C-4. Emitter Feedback With Drift-Offset Correction Current Source

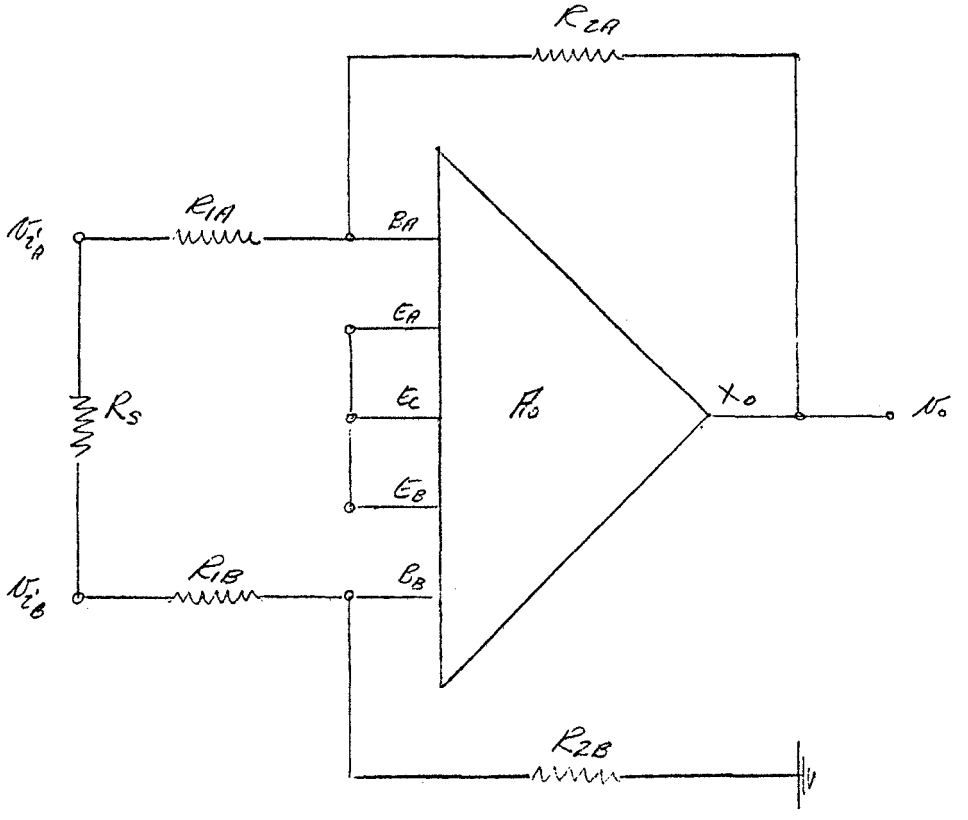


Figure C-5. Closed Loop Configuration With Base Feedback

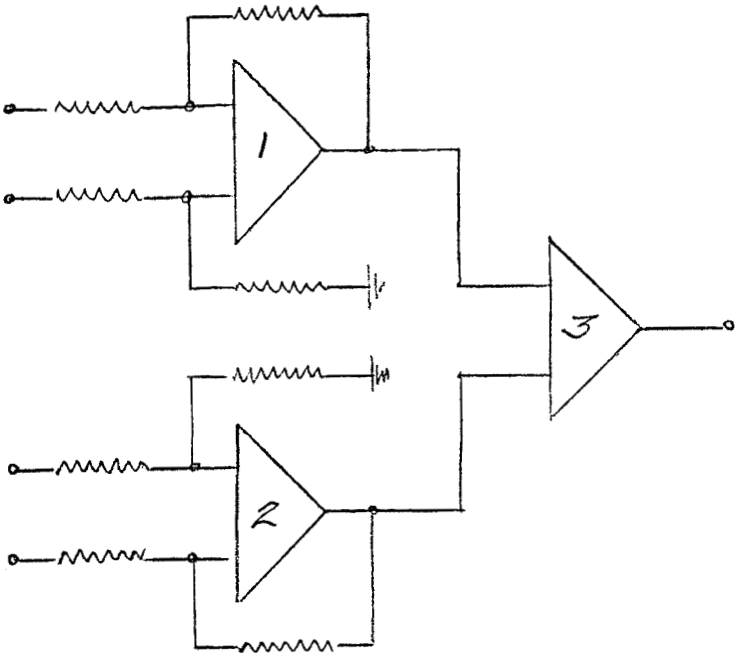


Figure C-6(a). Open-Loop High-Gain Amplifier Composite With Multiple Differential Inputs

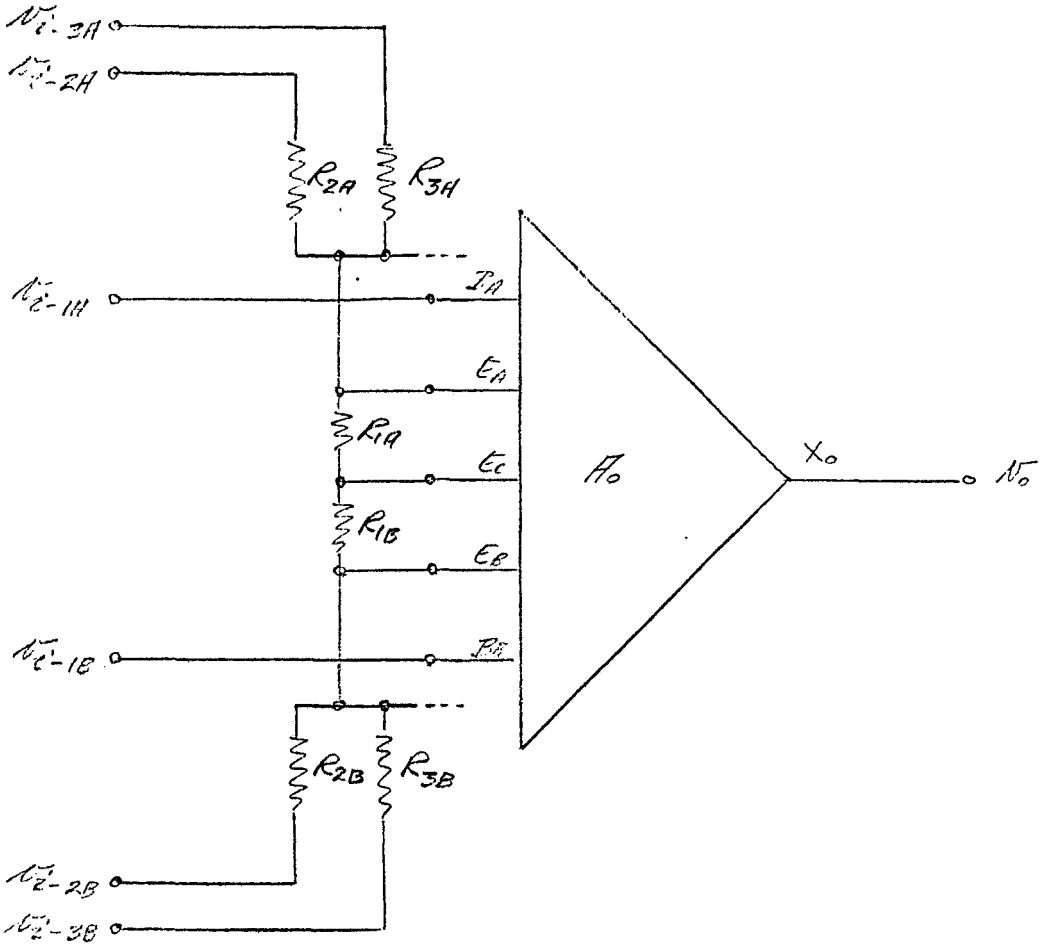


Figure C-6(b). MIA-101 Used as a Multiple Differential Input High-Gain Open-Loop Amplifier

converting a differential analog signal into a digital code. For instance, the MIA-101 becomes a differential comparator upon connecting the inputs as shown in Fig. C-7. In this configuration, inputs v_{i-A} and v_{i-B} are connected to the differential analog source voltage which is to be digitized. Resistor R_{2B} is grounded and resistor R_{2A} is connected to a variable reference voltage. The state of the output X_o is then determined by the relationship of the differential input signal to the variable reference voltage.

The equation describing the basic operation of this circuit is

$$v_o = \frac{R_o}{R_E (R_1 + R_2) + R_1 R_2} (v_{iA} - v_{iB})(R_1 + R_2) - R_1 (v_{XA} - v_{XB}) \qquad (25)$$

where R_E is given by Equation 14

$\frac{R_o}{R_E} = A_o$ (see Equation 15)

Equations 11 and 12 apply

$v_{XA} = E_R$

$v_{XB} = 0$

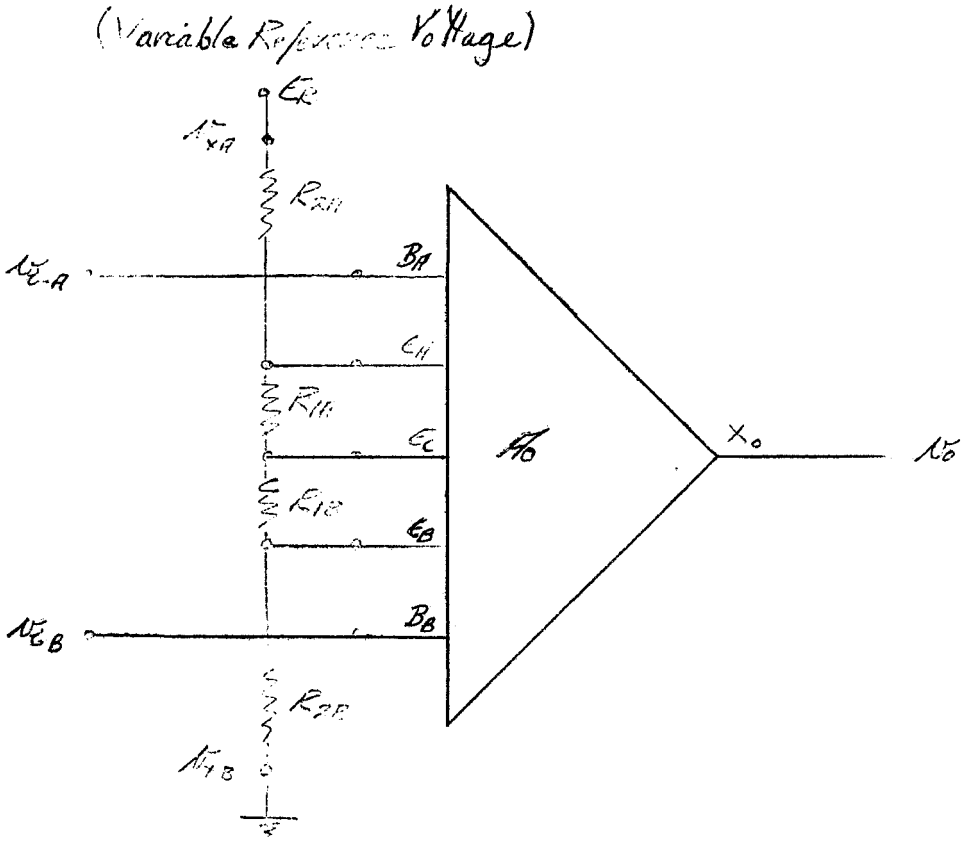


Figure C-7. Differential Comparator

APPENDIX D

PRINTED CIRCUIT BOARDS

The deliverable items on the Microminiature Signal Conditioner contract include five power sources and ten amplifiers. Each power source includes one DC-to-DC converter, one VR34 regulator, and two VR35 regulators. Each amplifier includes one SCA41 Basic Amplifier module, one CAP module for frequency compensation, and one SCA42 Drift-Offset Control module. A double-sided printed circuit board has been designed and fabricated to interconnect the above modules. The assembly drawing, front side metallization, and back side metallization are shown in Figures D-1, D-2, and D-3, respectively. Figures D-2 and D-3 show the boards with signal conditioning components.

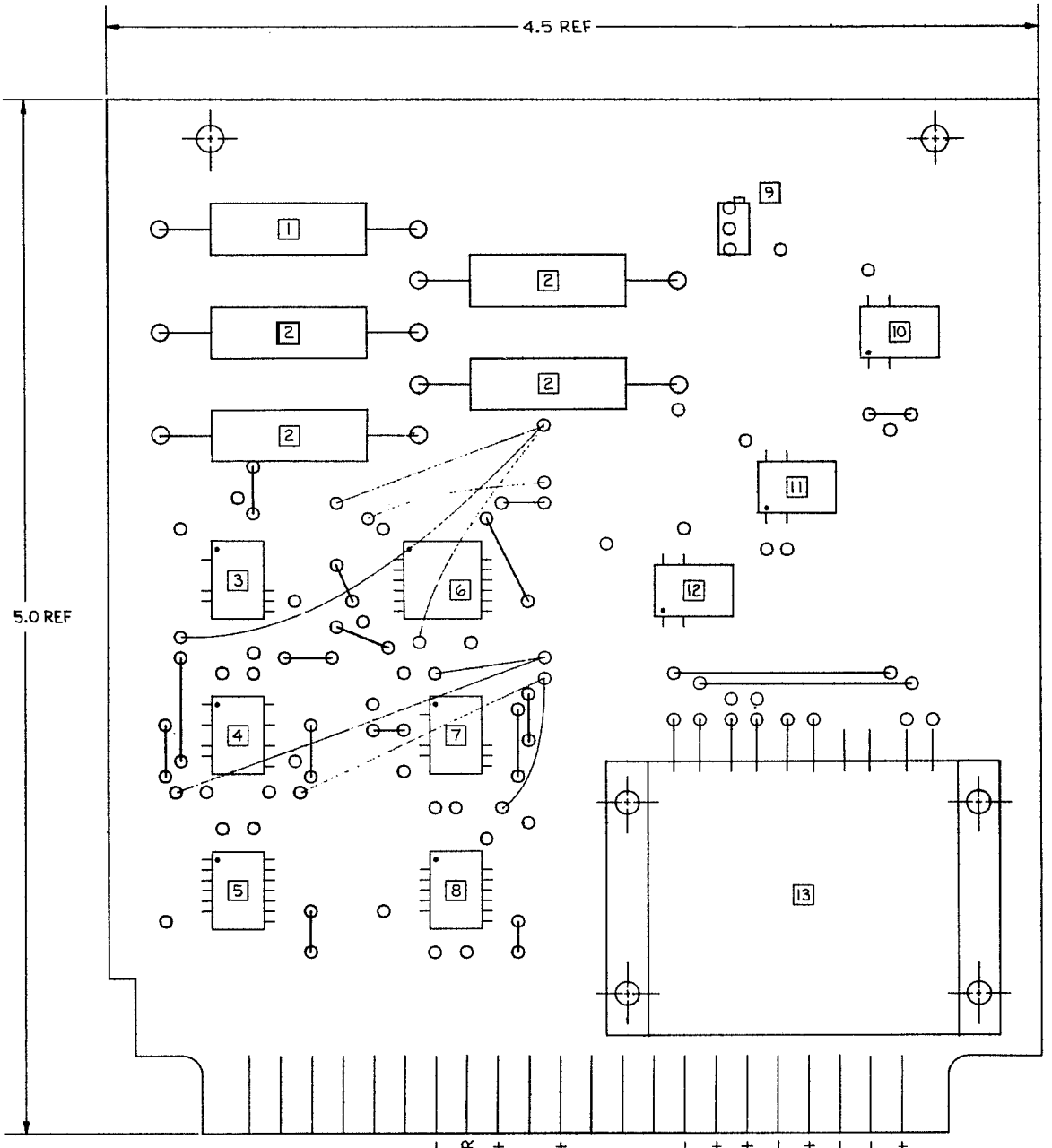
For contract delivery, five of these boards include the modules used in the power source. In this application, the amplifier module positions are left blank. Both the converter outputs and the series regulator outputs are available at the printed circuit card pin connections. A bridge adjust potentiometer and associated bridge resistors are included on the regulator boards. This loads each VR34 regulator with 360 ohms. Also, for contract delivery, ten of these boards contain amplifier modules. In this application the power source module positions are left blank. The printed circuit card is designed to accommodate one of the following three package configurations for the amplifier. Option A is used for this contract delivery to expedite the assembly and adjust phase.

Option A: Three separate packages
1. SCA41
2. CAP
3. SCA42

Option B: Two packages
1. SCA41 + CAP
2. SCA42

Option C: One package containing all die

This printed circuit card can be used later to interconnect a complete signal conditioning function, an amplifier and power source combined.



NOTES:
1. BRIDGE ADJUST
2. BRIDGE RESISTORS
3. SCA4-2 (X233757)
4. TWO CA-01'S (X223694)
5. SCA4-1 (X232884)
6. SCA4-1/SCA4-2/CA3-1
7. SCA 4-2
8. SCA4-1/TWO CA-01'S
9. BRIDGE ADJUST POTENTIOMETER
10. VR3-4 (X231932)
11. VR3-5 (X233756)
13. VR3-5
14. 3-WATT CONVERTER (X231447)
OR
(X235202)

Figure D-1. Printed Circuit Assembly
Signal Conditioner, Board No. 1

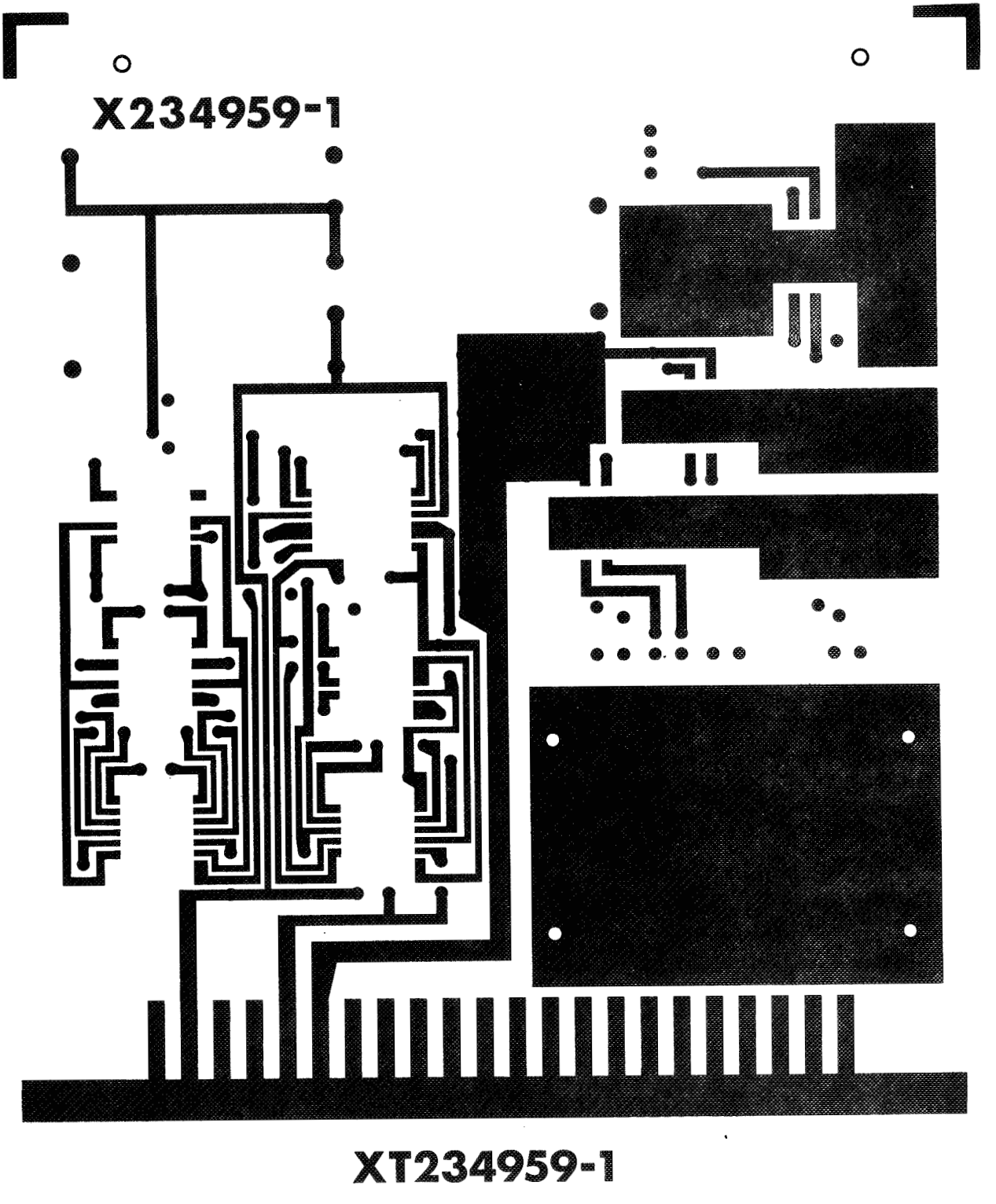
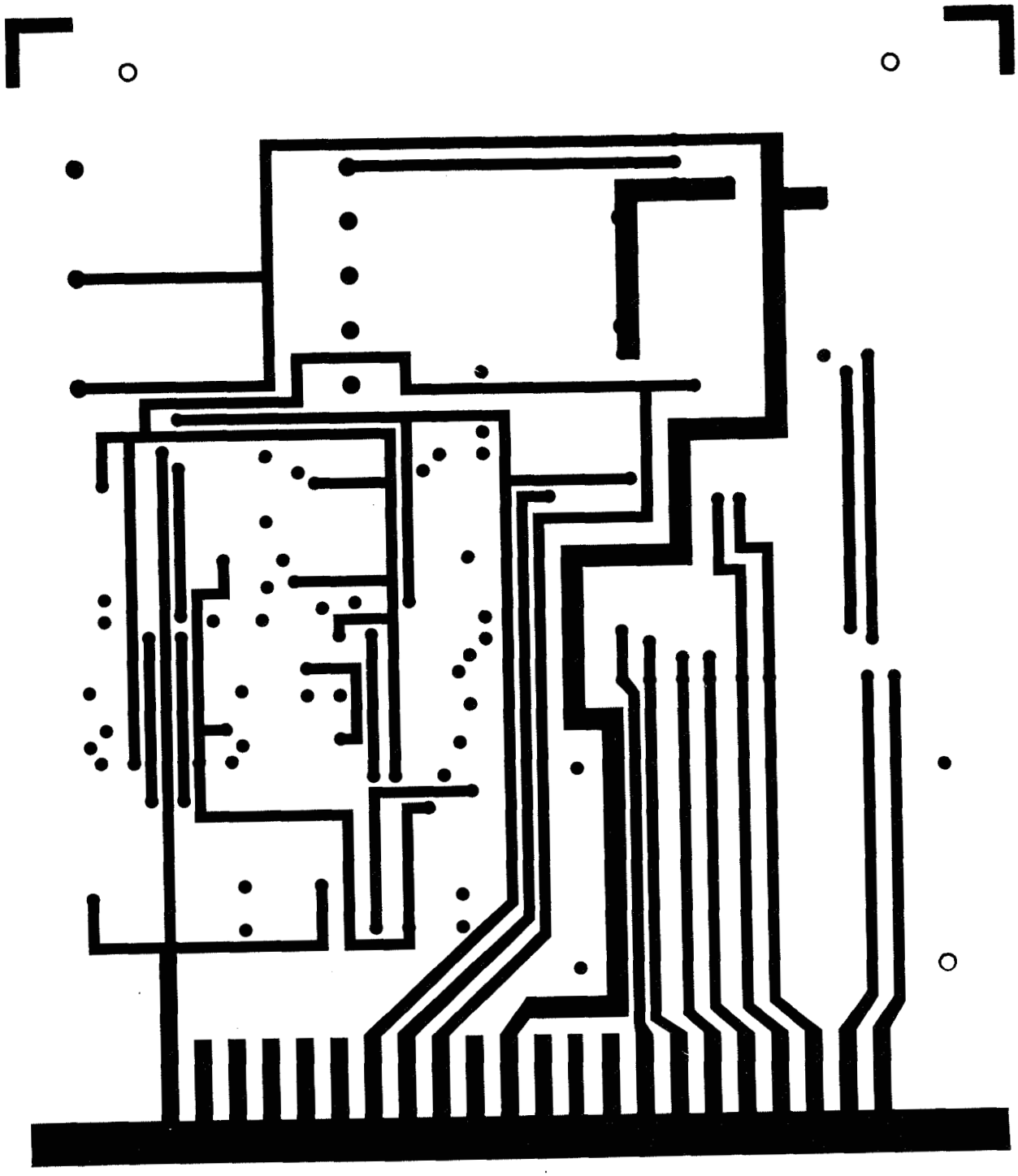


Figure D-2. Front Side, PC Board



XT234959-2

Figure D-3. Back Side, PC Board

APPENDIX E

NAS9-5293 POWER PROGRAMMER

Contract NAS9-5293 developed a microminiature 90-channel low-level signal conditioning system breadboard which features programmed power conditioning of 5 millivolt full scale analog signals and an IRIG specified PAM output. This sytem offers significantly reduced size, weight, and power combined with increased reliability over existing conventional low-level signal conditioning systems. A comparison is made in Table I.

TABLE I. COMPARISON OF CONVENTIONAL AND MICROMINIATURE 90-CHANNEL LOW-LEVEL SIGNAL CONDITIONING SYSTEMS

	Conventional	Microminiature	Reduction
Volume	750 in^3	< 50 in^3	> 93%
Weight	45 lbs	< 2 lbs	> 96%
Power	183 watts	5 watts	> 97%

Note: The microminiature volume and weight are estimates since system package design and fabrication were not included in this contract. The numbers refer to the complete system, including signal conditioners.

The system concept is made practical by the development of the monolithic integrated circuit, low-level dc amplifier under contract NAS9-3410. Adjustable evaporated cermet resistors on active silicon substrates, dielectric isolation, NPN-PNP transistors, MOSFET devices, MOS capacitors, and advanced circuit design techniques which incorporate these devices allow the system to be organized as described.

This contract includes the development and delivery of all circuits, except the signal modifiers, and includes a 12-channel breadboard model which demonstrates the operation of the system.

The system concept is illustrated in the block diagram of Figure E-1. The low-level transducer outputs range from 5 to 100 millivolts full scale. A signal modifier converts the output of a transducer into 0 to +5 volt full scale voltage. It may be dc amplifier, ac-to-dc converter, resistance-to-dc converter, or a phase-sensitive demodulator, depending upon the type of sensor.

Transducers, such as strain gauges, are sequentially energized via GTR gated voltage regulators. Power is likewise gated to signal modifiers, which are located on or near the transducers, via GMR gated voltage regulators. In the sequential mode of operation, all the channels are gated OFF at any one time, except the channel being monitored. This gating technique allows the system power input to be significantly decreased.

Since the maximum system sequencing rate is limited by the thermal-electrical settling time of the signal modifiers, provision is also made to gate ON the modifier and/or transducer power one sample time in advance. This optional increase in the maximum sequencing rate is accomplished at the expense of increased power input.

The outputs of the signal modifiers are multiplexed at a 0 to +5 volt full scale level and then conditioned into an IRIG specified PAM wavetrain by the output circuit. The control logic, which operates in one of two modes, sequential or random access, provides control signals to the analog switches, power switches, and output circuit. The power source converts a +28 volt unregulated battery voltage into four regulated dc voltages. It includes a microminiature pulse width modulated power converter.

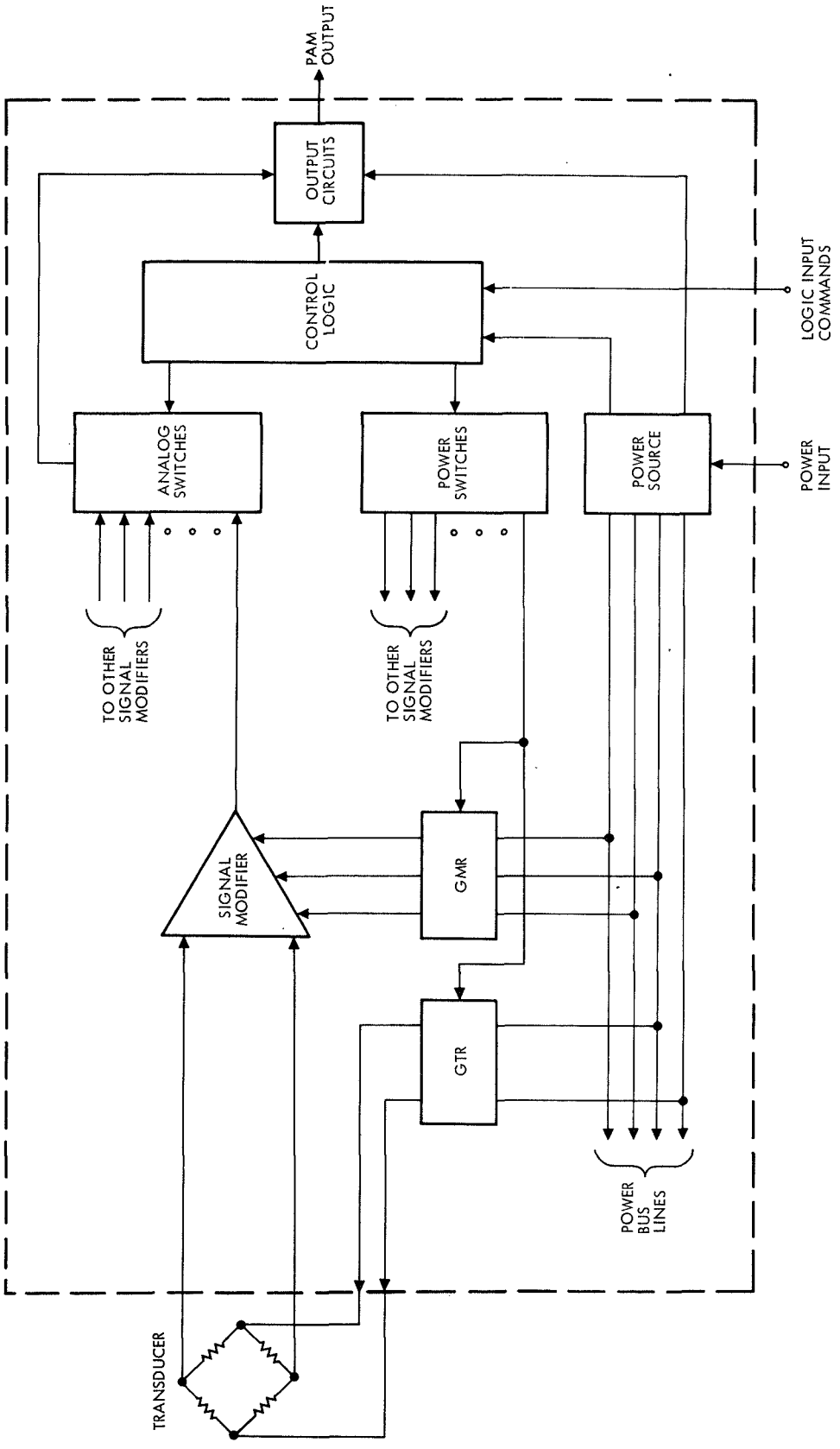


Figure E-1. Signal Conditioning System Block Diagram

Some of the inherent advantages of the described microminiature signal conditioning system are:

a) Low-level (5 millivolt full scale) inputs are conditioned.

b) Excitation power is supplied to transducers, such as strain gauges.

c) System power input is minimized by gating signal modifier and transducer power.

d) A signal modifier on each input channel provides flexibility in the type of analog signal to be conditioned.

e) A signal modifier on each analog input converts all signals to a high level before multiplexing, thereby minimizing analog errors normally encountered with long low-level signal lines and low-level multiplexers.

f) Crosstalk errors are minimized since all the channels are gated OFF at any one time, except the channel being monitored.

g) The maximum speed of the system can be increased by turning on each channel power in advance to the sample time.

APPENDIX F

POWER CONVERTER THERMAL ANALYSIS

A thermal analysis was performed on the power converter package.

Figures F-1 and F-2 show the heat dissipation calculations for the overall power converter package and the integrated circuit flat package. The analysis which follows is based on the information on the two figures. The results are summarized at the end.

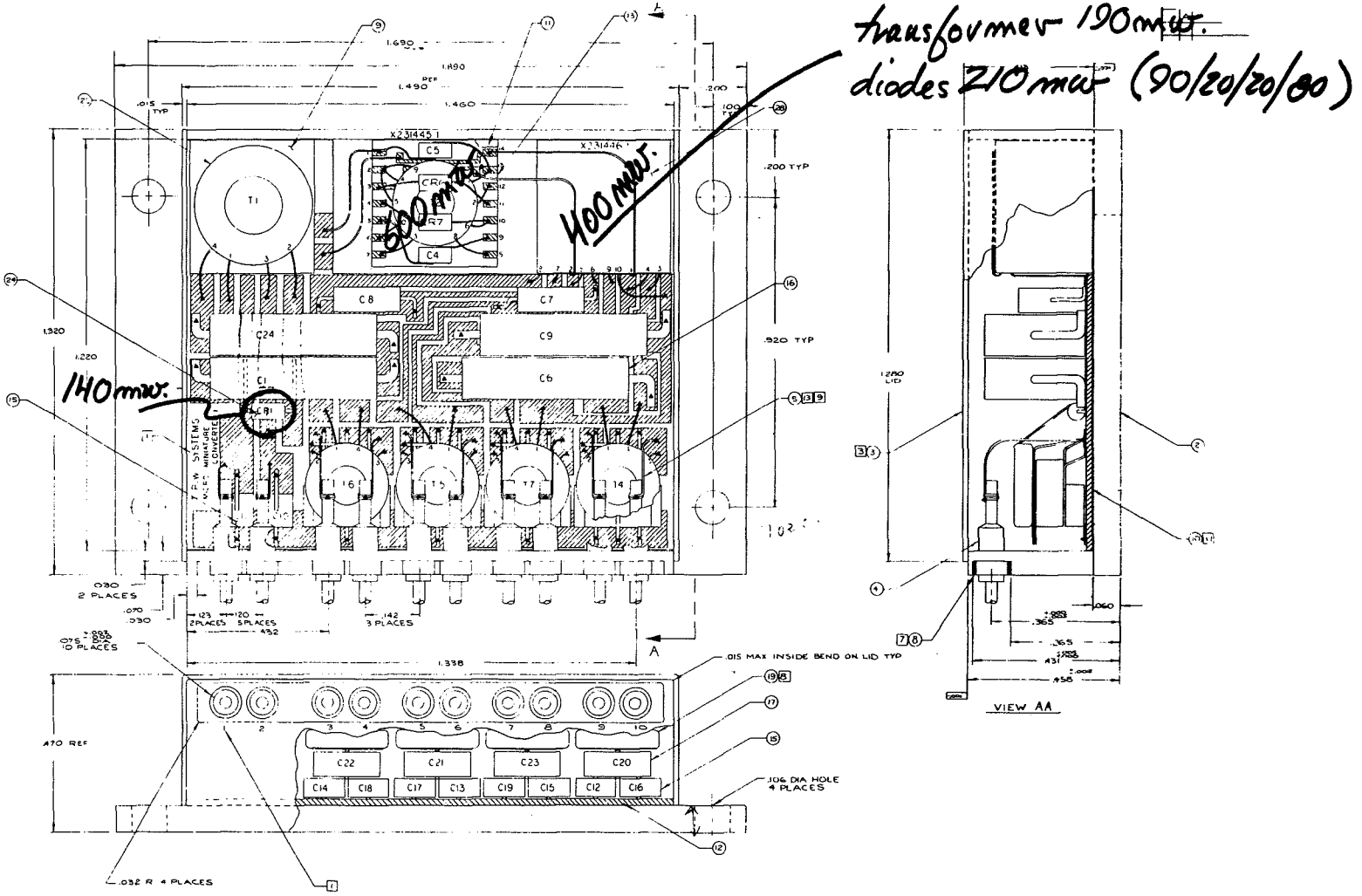


Figure F-1. Overall Package Heat Levels

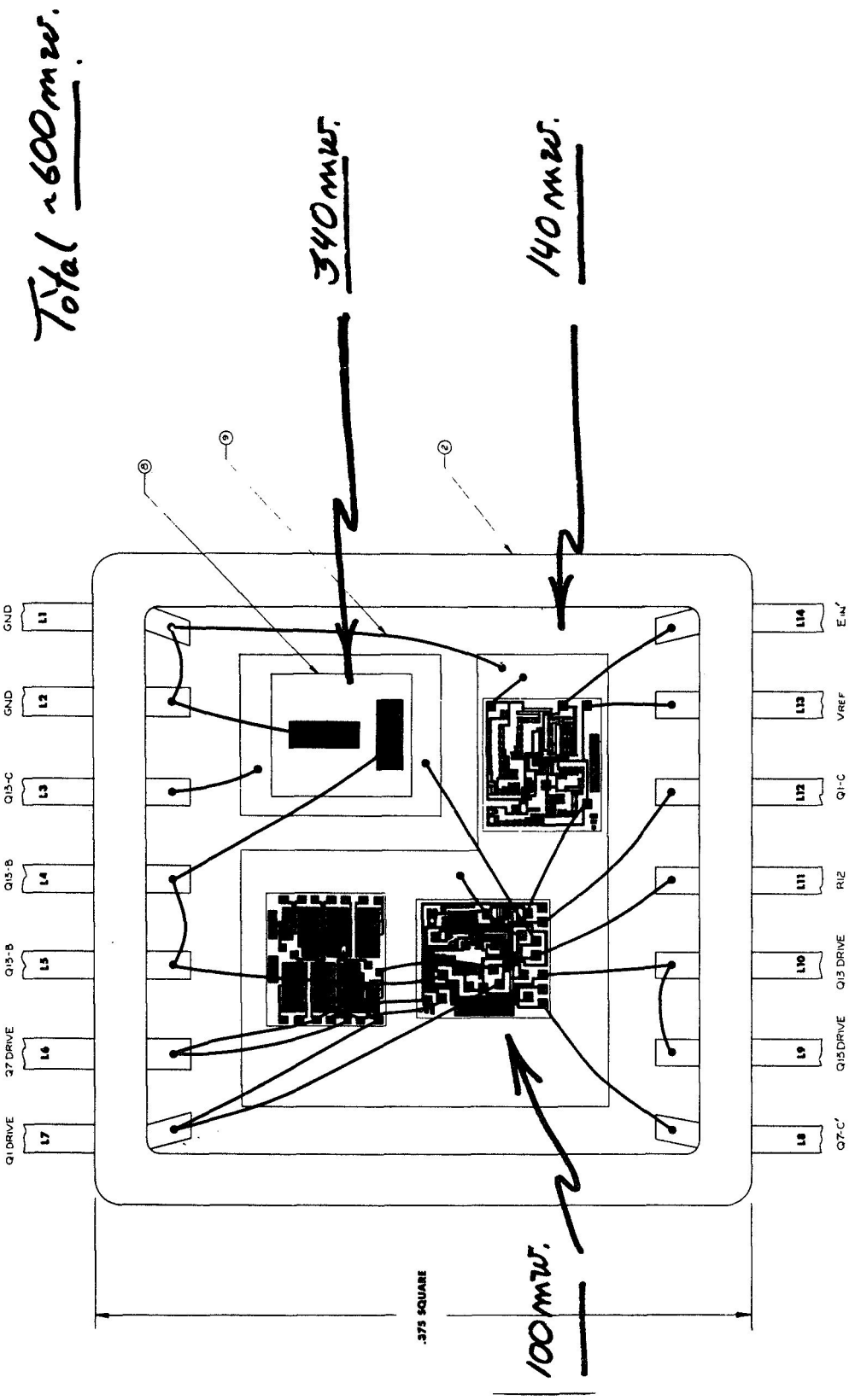
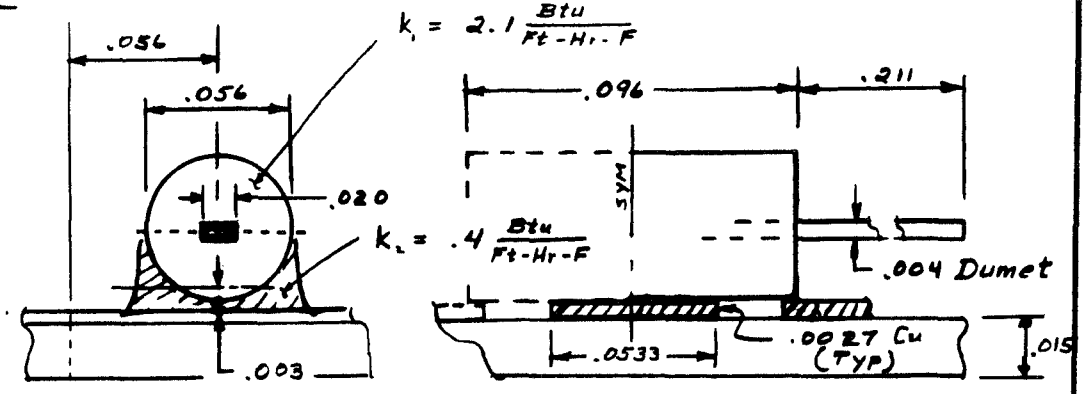


Figure F-2 Flat Package Heat Levels

TRW SYSTEMS		PREPARED BY: H. Lung
PROJECT	SUBJECT	DATE

CR 1



Assume an average gap of .003" between the case and the copper; diode is bonded to board with "Truecast".

Effective Area, $A_e = .866 \times .056 \times .096$

$$A_e = .00465 \text{ in}^2$$

$$R_1 = \frac{l_1}{k_1 A_e} = \frac{.028 \times 12}{2.1 \times .00465}$$

$$R_1 = 34.4 \frac{F}{Btu/Hr}.$$

$$R_2 = \frac{l_2}{k_2 A_2} = \frac{.003 \times 12}{.4 \times .056 \times .096}$$

$$R_2 = 16.8 \frac{F}{Btu/Hr}.$$

Case Resistance:

$$R_c = R_1 + R_2 = 51.2 \frac{F}{Btu/Hr}.$$

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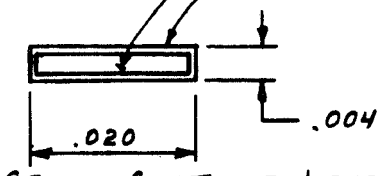
$k = 7.26 \frac{Btu}{Hr\text{-}Ft\text{-}F}$

75% (42% Ni, 58% Fe)

25% Cu $k = 220 \frac{Btu}{Hr\text{-}Ft\text{-}F}$.



CROSS SECT. OF LEAD

$A = .020 \times .004 = .00008 in^2$

$$R_3 = \frac{.211 \times 12}{7.26 \times .75 \times .00008} = 5810 \frac{F}{Btu/Hr}.$$

$$R_4 = \frac{.211 \times 12}{220 \times .25 \times .00008} = 575 \frac{F}{Btu/Hr}.$$

Lead Resistance :

$$R_L = \frac{R_1 R_2}{R_1 + R_2} = 524 \frac{F}{Btu/Hr}.$$

Calculated Conductivity of Dumet with pure copper :

$k = 60 \frac{Btu}{Hr\text{-}Ft\text{-}F}$.

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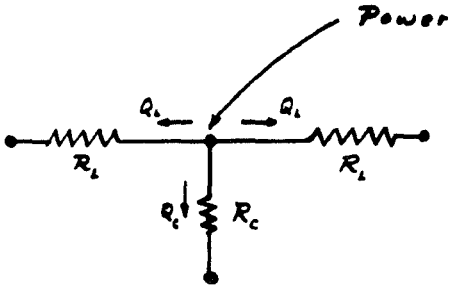

① $2Q_L + Q_c = Q_T$

② $Q_L R_L = Q_c R_c$

Substituting ① into ②:

$$Q_L R_L = (Q_T - 2Q_L) R_c$$

$$Q_L = \frac{Q_T R_c}{R_L + 2R_c}$$

$$Q_L = \frac{.477 \times 51.2}{524 + (2 \times 51.2)}$$

$$Q_L = .039 \text{ Btu/Hr.}$$

$$Q_c = .477 - 2Q_L$$

$$Q_c = .40 \text{ Btu/Hr.}$$

Temp. Drop across the diode case is assumed equal to the ΔT through each of the two Dumet leads.

$$\Delta T_1 = Q_L R_L = Q_c R_c$$

$$\Delta T_1 = .40 \times 51.2 = 20.5 \text{ F.}$$

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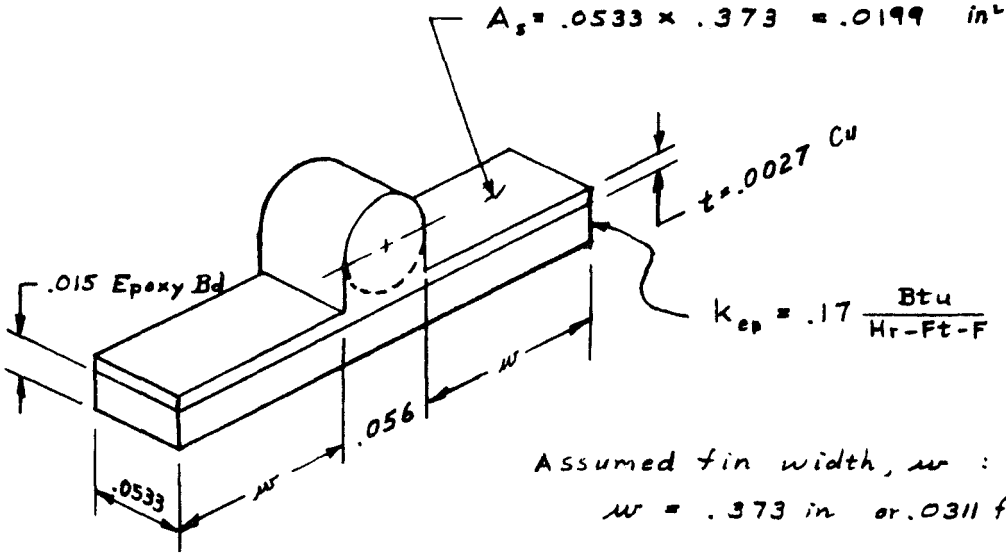


Assumed fin width, w :

w = .373 in or .0311 ft

For constant heat flux through the epoxy bd. & copper:

$$R = \frac{.0027 \times 12}{226 \times .0199} + \frac{.015 \times 12}{.17 \times .0199} = .0072 + 53.2$$

$$R = 53.2 \frac{F}{Btu/Hr} .$$

$$h = \frac{1}{RA_s} = \frac{144}{53.2 \times .0199}$$

$$h = 136 \frac{Btu}{Hr-Ft^2-F} .$$

Fin efficiency :

Ref (1)

$$\eta = \frac{\tanh w\sqrt{\frac{h}{kt}}}{w\sqrt{\frac{h}{kt}}}$$

$$w\sqrt{\frac{h}{kt}} = .0311\sqrt{\frac{136}{226 \times .000225}} = 1.61$$

$$\eta = \frac{\tanh 1.61}{1.61} = \frac{.92316}{1.61}$$

$$\eta = 57.3\ \%$$

Equivalent fin size with same temp. as root temp.

$A_p = .373 \times .0533 = .0199 \text{ in}^2$

$57.3\% A_p = .0114 \text{ in}^2$

Equiv. width, w_e

$$w_e = \frac{.0114}{.053} = .215 \text{ in.}$$

Equiv. surface area of constant temp.

$[(2 \times .215) + .056].0533 = .0259 \text{ in}^2$

Actual Resistance across the epoxy bd. & copper:

$$R = \frac{.0027 \times 12}{226 \times .0259} + \frac{.015 \times 12}{.17 \times .0259} = 40.8 \frac{F}{Btu/Hr}.$$

$Q_c = .40 \text{ Btu/Hr}$

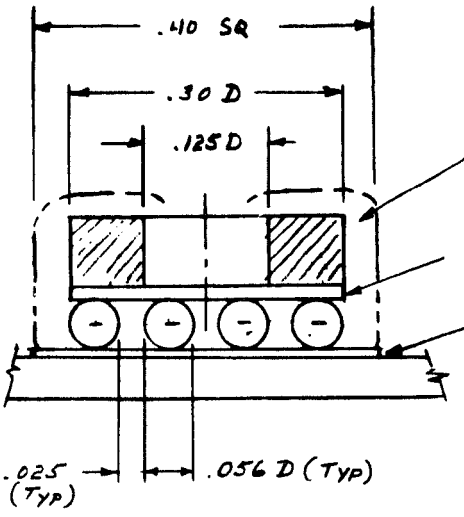
$\Delta T_2 = Q_c R = 16.4 \text{ F.}$

Total temp rise from jct. pt. of CR-1 to Alum. ℄:

$\Delta T_T = \Delta T_1 + \Delta T_2 = 20.5 + 16.4$

$\Delta T_T = 36.9 \text{ F.} \quad \text{or} \quad 20.5 \text{ C.}$

XFMR



Transformer Core Resistance is combined resistances along 3 thermal paths.

R_1 is thru mylar and diode.

R_2 is thru mylar and "Truecast" (between diodes).

R_3 is thru "Truecast" (via periphery).

Path 1 (to ctr of diode):

$$R_1 = \sum \frac{l}{kA} = \frac{.005 \times 12}{.087 \times .056 \times .096} + \frac{.028 \times 12}{2.1 \times .00465}$$

$$+ \frac{.010 \times 12}{.40 \times .056 \times .096} \quad \text{(Note: for 1/2 path)}$$

$$R_1 = \tfrac{1}{2}(128.4 + 34.4 + 55.8) = 109.3 \ \frac{F}{Btu/Hr}.$$

Path 1' (ctr of diode to alum. base):

$$R_1' = \frac{.028 \times 12}{2.1 \times .00465} + \frac{.010 \times 12}{.40 \times .056 \times .096} + \frac{.003 \times 12}{.10 \times .056 \times .096}$$

$$R_1' = 157.2 \ \frac{F}{Btu/Hr}. \quad \text{(Note: for 1/2 path)}$$

$$R_1' = 78.6 \ \frac{F}{Btu/Hr}.$$

Path 2 :

Effective Area, $A = .785(D_o^2 - D_i^2) - 2(.056 \times .096)$

$A = .0584 - .01075 = .0476\ in^2$

$$R_2 = \sum \frac{1}{kA} = \frac{.005 \times 12}{.087 \times .0476} + \frac{.056 \times 12}{.40 \times .0476} + \frac{.003 \times 12}{.10 \times .0476}$$

$R_2 = 14.5 + 35.2 + 7.56$

$R_2 = 57.3 \frac{F}{Btu/Hr}$.

Path 3 :

$A_1 = \pi(.40)(.0875) = .11\ in^2$

$A_2 = (.40)^2 - .785(.30)^2 = .09\ in^2$

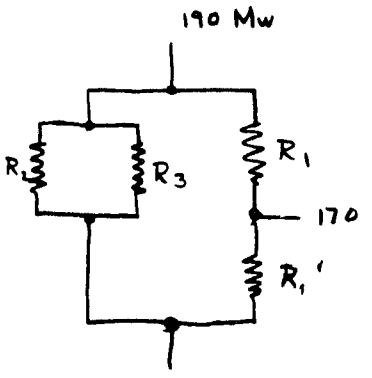
$$R_3 = \frac{.05 \times 12}{.40 \times .11} + \frac{.105 \times 12}{.40 \times .09} + \frac{.003 \times 12}{.10 \times .09}$$

$R_3 = 13.6 + 35.0 + 4.0$

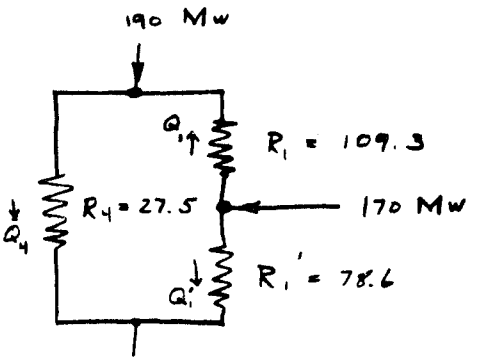
$R_3 = 52.6 \frac{F}{Btu/Hr}$.

Combining Resistances, R_2 & R_3 into R_4 :

$$R_4 = \frac{R_2 R_3}{R_2 + R_3} = \frac{3020}{109.9} = 27.5 \frac{F}{Btu/Hr}$$



Equiv. Circuit



Modified Circuit

Using Modified Circuit :

$$Q_1' R_1' = Q_1 R_1 + (Q_1 + 190) R_4$$

$$Q_1' + Q = 170 \quad \text{or} \quad Q_1' = 170 - Q_1$$

$$(170 - Q_1) R_1' = Q_1 R_1 + Q_1 R_4 + 190 R_4$$

$$Q_1 = \frac{170 R_1' - 190 R_4}{R_1 + R_4 + R_1'} = \frac{170 \times 78.6 - 190 \times 27.5}{109.3 + 27.5 + 78.6}$$

$Q_1 = 37.8$ Mw or .13 Btu/Hr.

$Q_1' = 170 - 37.8 = 132.2$ Mw or .45 Btu/Hr

$Q_4 = Q_1 + 190 = 227.8$ Mw or .776 Btu/Hr

$\Delta T_1' = R_1' Q_1' = 78.6 \times .45 = 35.4$ F (19.6 C)

$\Delta T_4 = R_4 Q_4 = 27.5 \times .776 = 21.4$ F (11.9 C)

$\Delta T_1 = R_1 Q_1 = 109.3 \times .13 = 14.2$ F (7.9 C)

∴ Junction temp. of diode is :

$\Delta T_1' = 35.4$ F. or 19.6 C.

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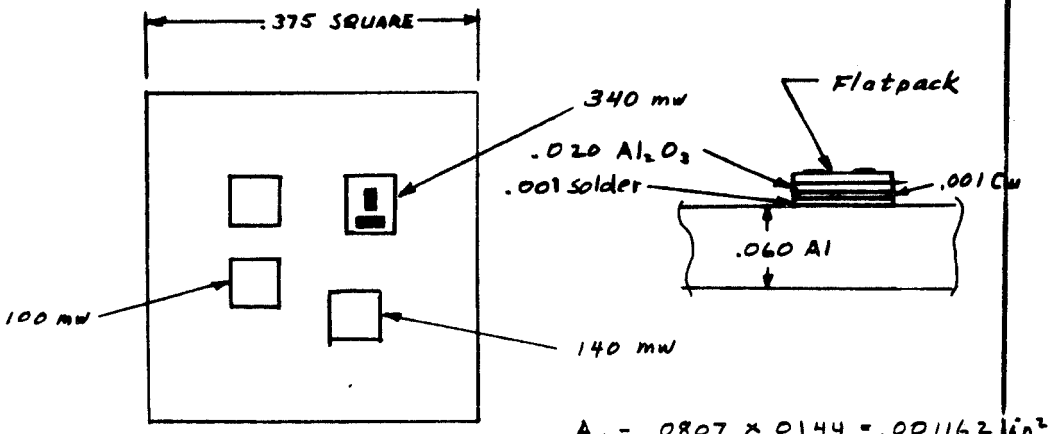
FLATPACK



$A_c = .0807 \times .0144 = .001162 \text{ in}^2$

$k_{Al_2O_3} = 10.7 \frac{Btu}{Hr\text{-}Ft\text{-}F}$.

$k_{solder} = 14$ " .

$k_{cu} = 222$ " .

Typical Resistance per flatpack:

$$R = \sum \frac{l}{kA_c} = \frac{12}{.001162}\left(\frac{.020}{10.7} + \frac{.001}{222} + \frac{.001}{14}\right)$$

$R = 2.66 \frac{F}{Btu/Hr}$.

$Q = .340 \times 3.413 = 1.16 \text{ Btu/Hr}$

$\Delta T = QR = 3.1$ F. or 1.7 C.

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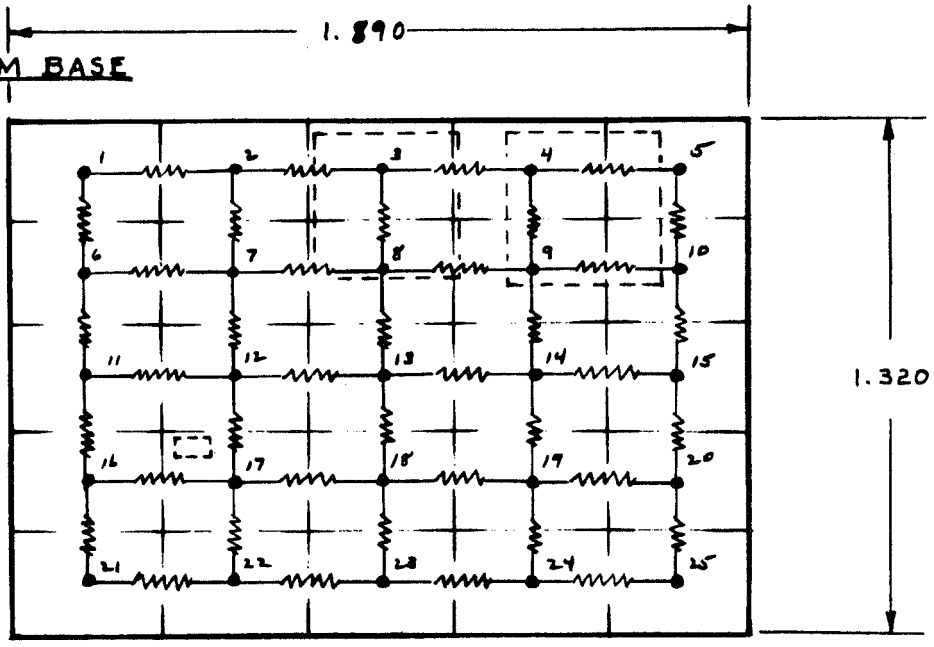
ALUMINUM BASE



Conductances, Resistances:

1-2, 2-3, 3-4, 4-5, 6-7, 7-8, 8-9, 9-10, 11-12, 12-13, 13-14, 14-15, 16-17, 17-18, 18-19, 19-20, 21-22, 22-23, 23-24, 24-25

(across) $K = \frac{kA}{l} = \frac{100 \times .06 \times .364}{12 \times .378} = .35$ Btu/Hr-F.

$R = K^{-1} = 2.86 \frac{F-Hr}{Btu}$.

1-6, 6-11, 11-16, 16-21, 2-7, 7-12, 12-17, 17-22, 3-8, 8-13, 13-18, 18-23, 4-9, 9-14, 14-19, 19-24, 5-10, 10-15, 15-20, 20-25

(down) $K = \frac{100 \times .06 \times .378}{12 \times .264} = .716$ Btu/Hr-F.

$R = 1.397 \frac{F-Hr}{Btu}$.

Heat Input:

Node 3 $Q_3 = .340 \times 3.413 = 1.16$ Btu/Hr.

Node 8 $Q_8 = .260 \times 3.413 = .887$ "

Node 4 $Q_4 = 3/5 (.2 \times 3.413) = .41$ "

Node 9 $Q_9 = 3/5 (.2 \times 3.413) = .41$ "

Node 5 $Q_5 = 2/5 (.2 \times 3.413) = .273$ Btu/Hr.

Node 10 $Q_{10} = 2/5 (.2 \times 3.413) = .273$ "

Node 17 $Q_{17} = .14 \times 3.413 = .477$ "

Interface Resistance:

Assume interface conductivity

$$h = 200 \frac{\text{Btu}}{\text{Hr-Ft}^2\text{-F}}.$$

$$\mathcal{R} = \frac{1}{hA} = \frac{144}{200 \times .264 \times .378}$$

$$\mathcal{R} = 7.2 \frac{\text{F}}{\text{Btu/Hr}}.$$

Subsequent table of node temperatures were obtained from a Thermal Circuit Analyzer.

Temperature Rise of Nodes from Infinite Heat Sink

Node	ΔT (F)	Node	ΔT (F)
1	.8	13	1.2
2	1.2	14	1.1
3	2.4	15	1.1
4	2.0	16	.3
5	1.7	17	.8
6	.7	18	.8
7	1.0	19	.8
8	2.0	20	.8
9	1.7	21	0
10	1.5	22	.5
11	.5	23	.7
12	.9	24	.7
		25	.7

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Max. temp. rise for CR-1 :

$\Delta T = 36.9 + .8 = 37.7$ F.

$\Delta T = 20.9$ C.

Max. temp. rise for flatpack:

$\Delta T = 3.1 + 2.4 = 5.5$ F.

$\Delta T = 3.1$ C.

Max. temp. rise for Xfmr :

$\Delta T = 35.4 + 1.7 = 37.1$ F.

$\Delta T = 20.6$ C.

References :

(1) "Conduction Heat Transfer", P. J. Schneider, Addison - Wesley, 1957, p. 73.

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